RTL though OS

Goal: Demonstrate mastery of computer engineering by designing and implementing a single core RISC-V processor and developing a basic multitasking kernel to run on the processor.

Team

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Why?

- Synthesizing 18-447 and 15-410 will help us develop an understanding of the interface between hardware and software
- We want to experience the thrills of debugging a system with neither a ground truth software implementation nor a ground truth hardware implementation
- We want to develop a unique skill set that spans both kernels and processors.

Outline:

- Processor
    - We will design and implement a single core RISC-V processor with the RV32I-MA specification.
        - User mode version 2.2
        - Privileged Architecture version 1.10
        - https://riscv.org/specifications/
- Kernel
    - We will develop a kernel to run on our RISC-V processor with the Pebbles kernel spec
        - http://www.cs.cmu.edu/~410/p2/kspec.pdf
- Platform
    - We will deploy both the processor and the kernel on an FPGA. This will require a VGA display and keyboard input over PS/2.
        - Our FPGA platform will require 20k LUTs, 10k FFs, 12 BRAMs (36Kib block). These resource utilizations are rather small and we could deploy on a wide range of FPGAs. Thus our selection process for FPGA is primarily based on the peripheral support since we desire a VGA output and a PS/2 input. We also require ~64 MB of DRAM to support regular application usage.
            - https://carrv.github.io/papers/matthews-taiga-carrv2017.pdf
- Evaluation
    - We have a target suite of programs that we want to run on our kernel successfully, which test a large amount of the system but not necessarily achieve 100% test coverage of hardware. For the demo day we will have a wide variety of games that can be played.
    - In addition, we will have specific unit tests for the hardware, as well as constrained random testing to increase the confidence in our design.