Final Review

Recitation 10

Logistics

- Dec 7th - Final Exam
- Dec 7th 9:30 am- HW 10 Due
- Dec 7th 9:30 am - Lab 5 Due
  - Dec 13 11:59 pm Drop Dead Deadline. NO EXCEPTIONS!
- Monday Dec 3, Extra OH 2-4pm and 4-6pm

Virtual Memory

- VM <-> Data Cache Interactions
  - VIPT, VIVT, PIPT Caching
- Hierarchical Page Tables
- Alternative Page Tables (Unified, Hashed, etc).
- TLB
  - TLB <-> Cache relationship
  - TLB Impact on AMAT
- VM performance metrics (Utilization, Translation Speed, AMAT etc.)

Cache Coherency

- MSI State Transitions
  - Performance Metrics, Bus Utilization, Data Movement, Hit Rate.
- Directory Based Cache Coherency
- Cache Coherence Requirements
  - SWMR Invariant
  - Write Serialization
- Cache Coherence -> Memory Consistency Relation

Memory Consistency

- Memory Coherence VS Memory Consistency
- Sequential Consistency
- Weaker Consistency Models
  - TSO and PSO
- Strong Consistency Models
  - Strict consistency
- Enforcing Sequential consistency (adding Fences)
- Ordering, and possible Executions

Synchronization and Atomicity

- Atomic Operations
- Transactional memory

Propagation Blocking

- Ideal Candidates for Binning
- T-Opt and P-Opt Replacement
- Relationships between Bin size and Cache configurations

Advanced Architecture

- Multi-Core Interconnects
  - Mesh Networks, Trees, Rings…
  - Scalability (Resource utilization, Performance Metrics)
- Speculative Attacks
  - Branch Speculation Attacks
  - Cache Timing Attacks
  - Side - Channel Attacks
  - Relationship to Visible State (ISA)