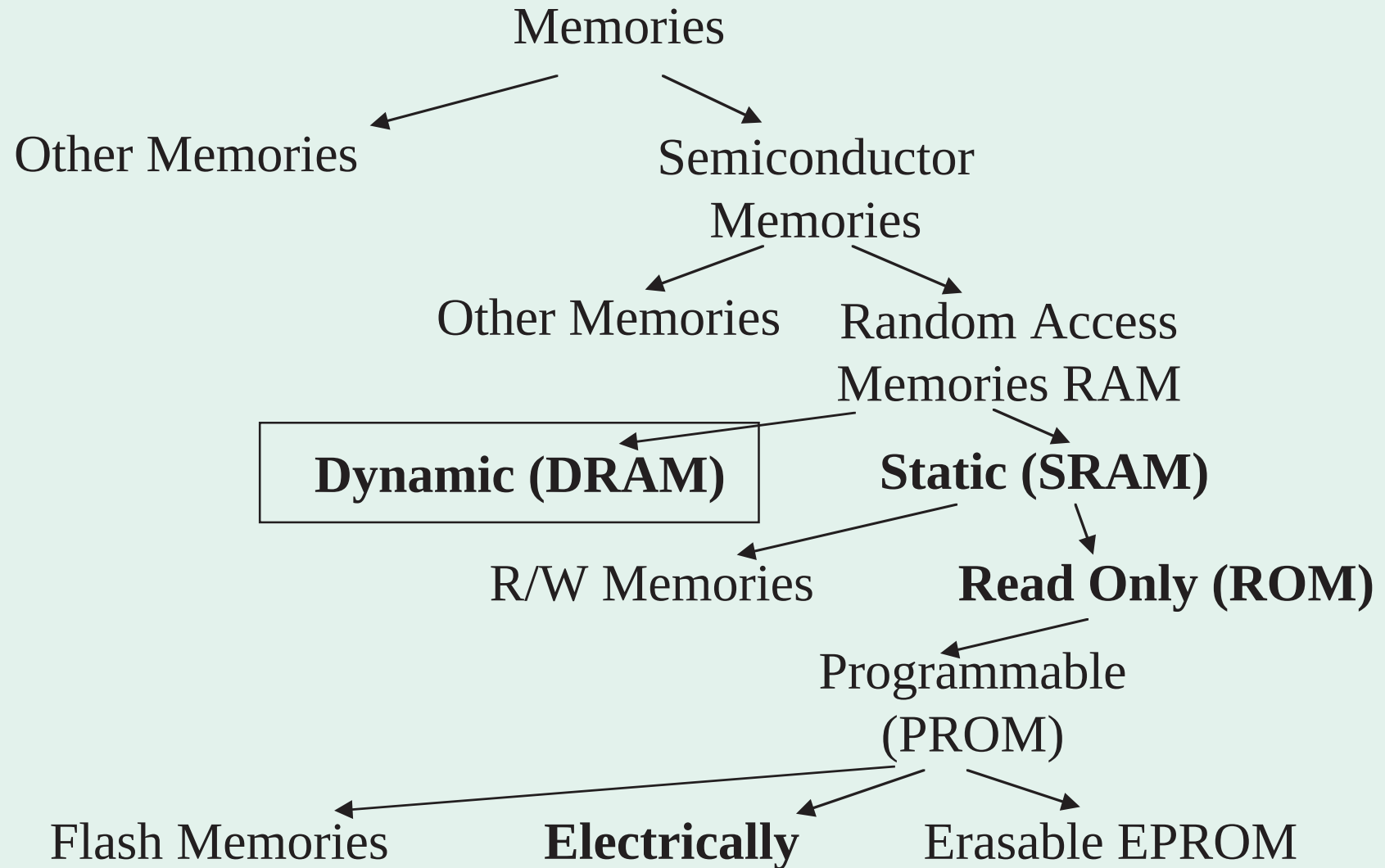


Memory III: Dynamic Random Access

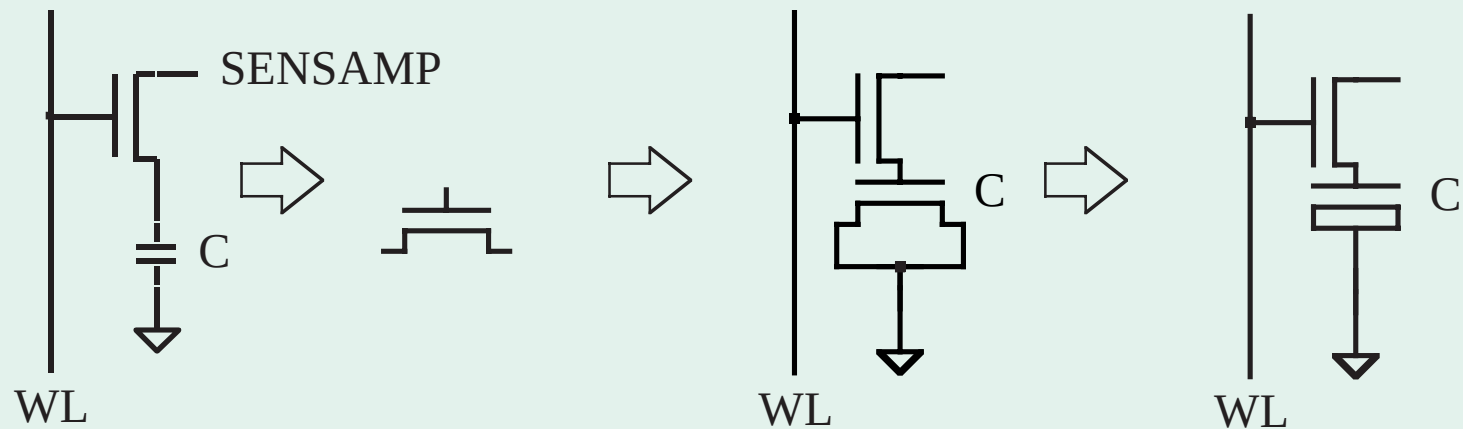
- **Memory Classification**
- **DRAM basics**
 - Single transistor memory cell
 - Memory architecture
- **DRAM circuitry**
 - Read/refresh operation
 - Charge sharing
 - DRAM design trends/limitations

Memory Classification



DRAM basics

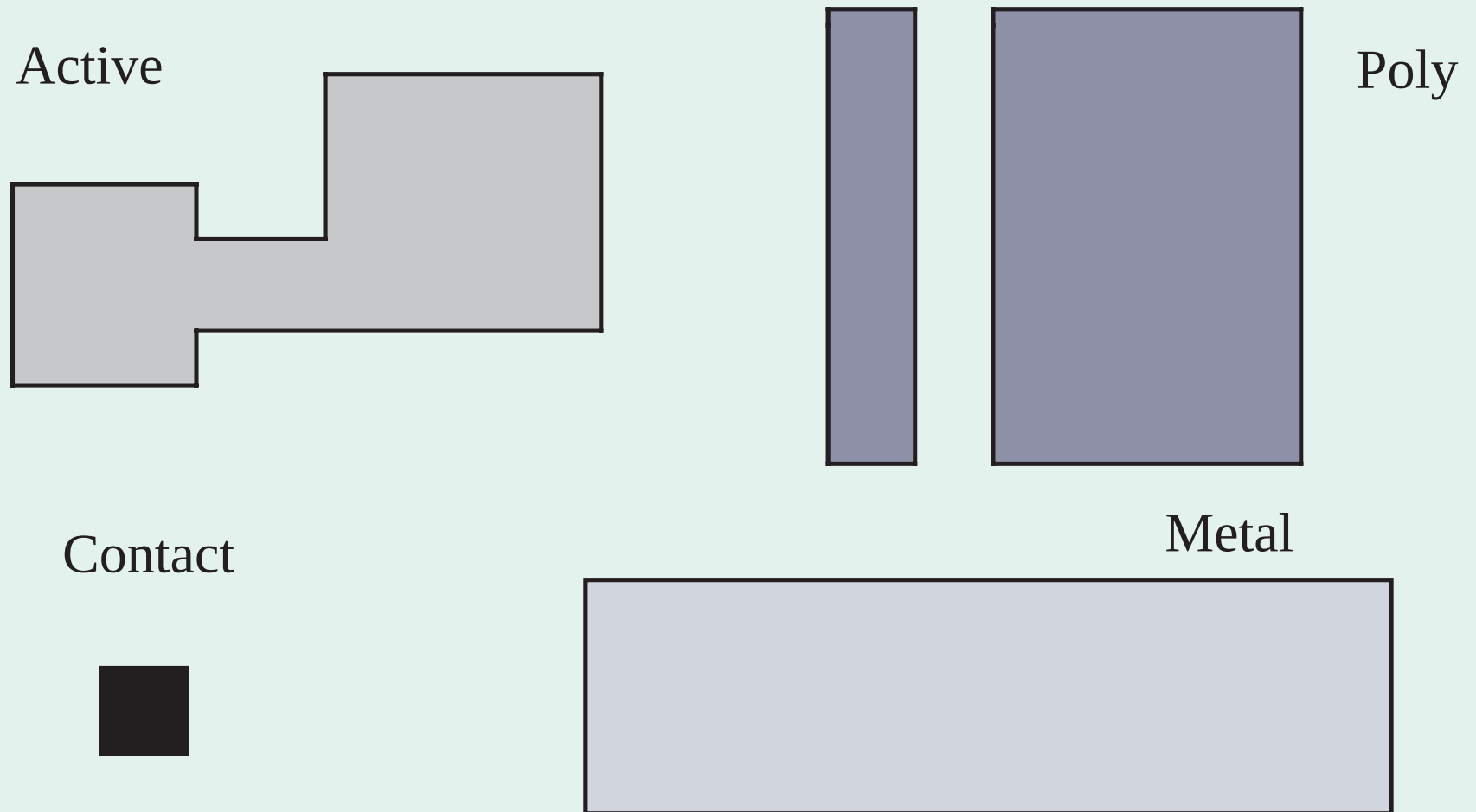
Single transistor memory cell



Leakage !

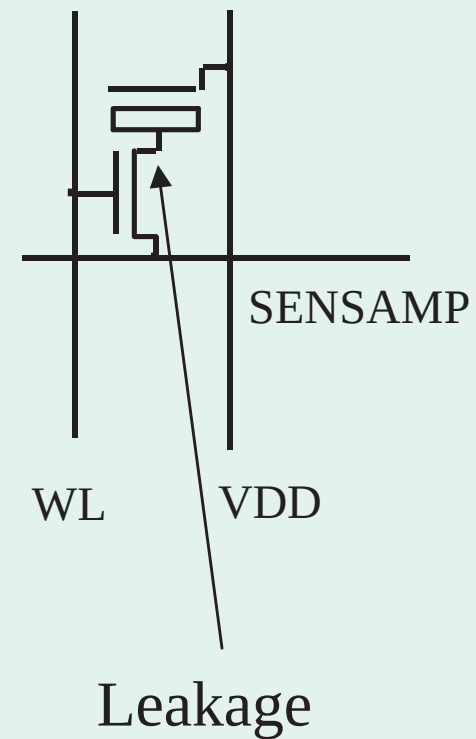
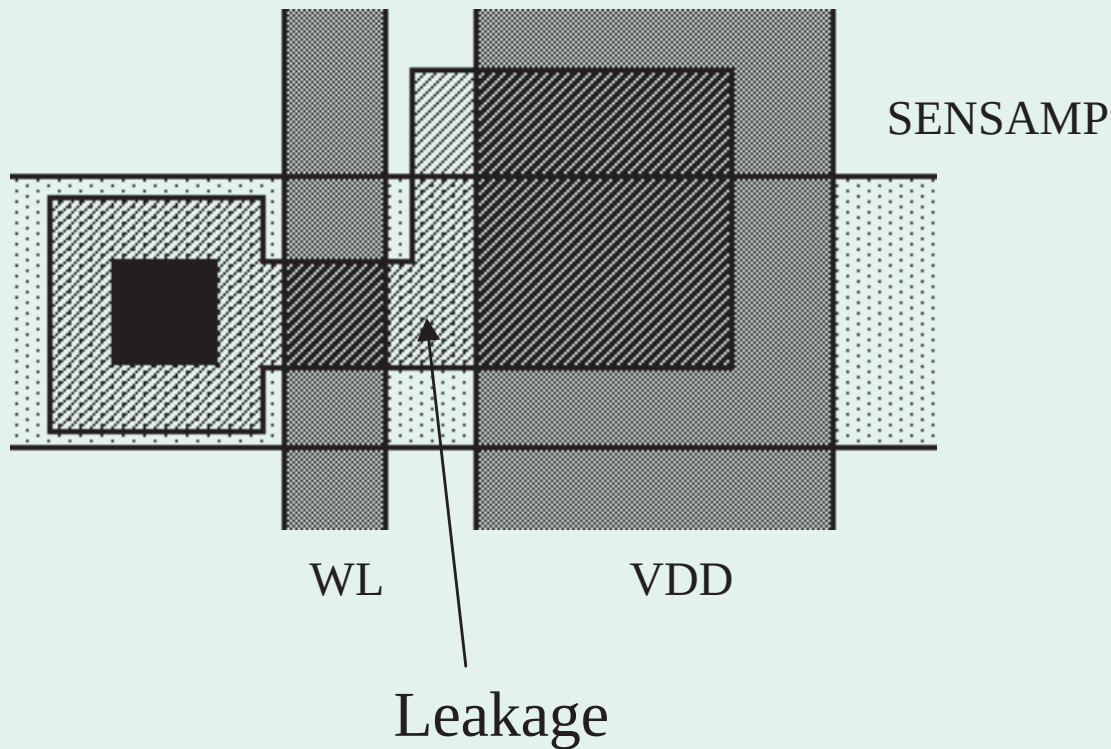
DRAM basics

Single transistor memory cell



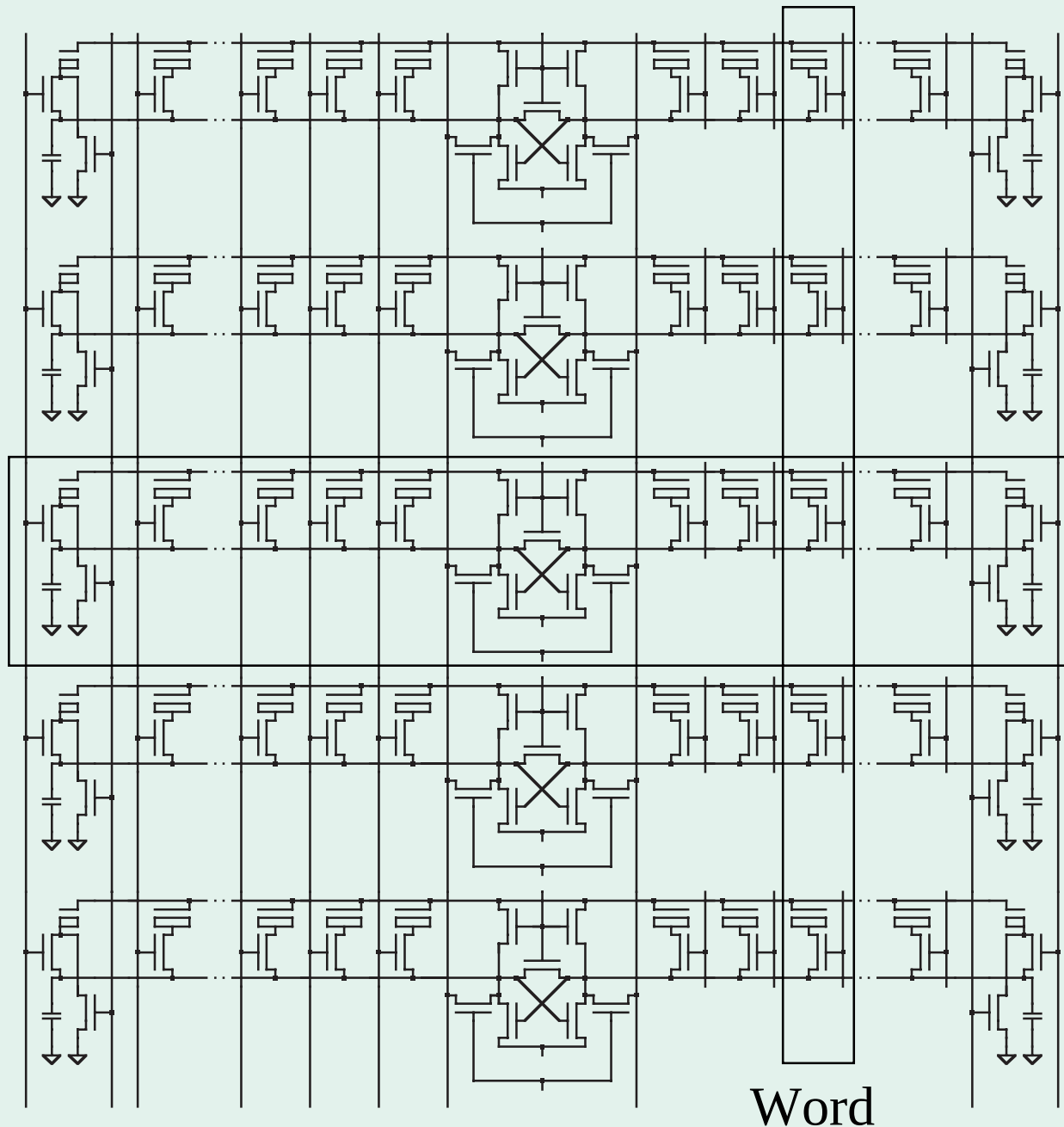
DRAM basics

Single transistor memory cell



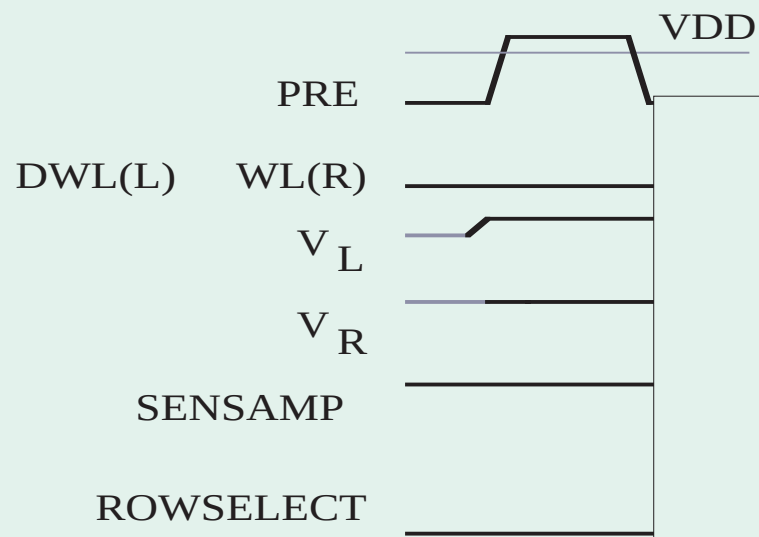
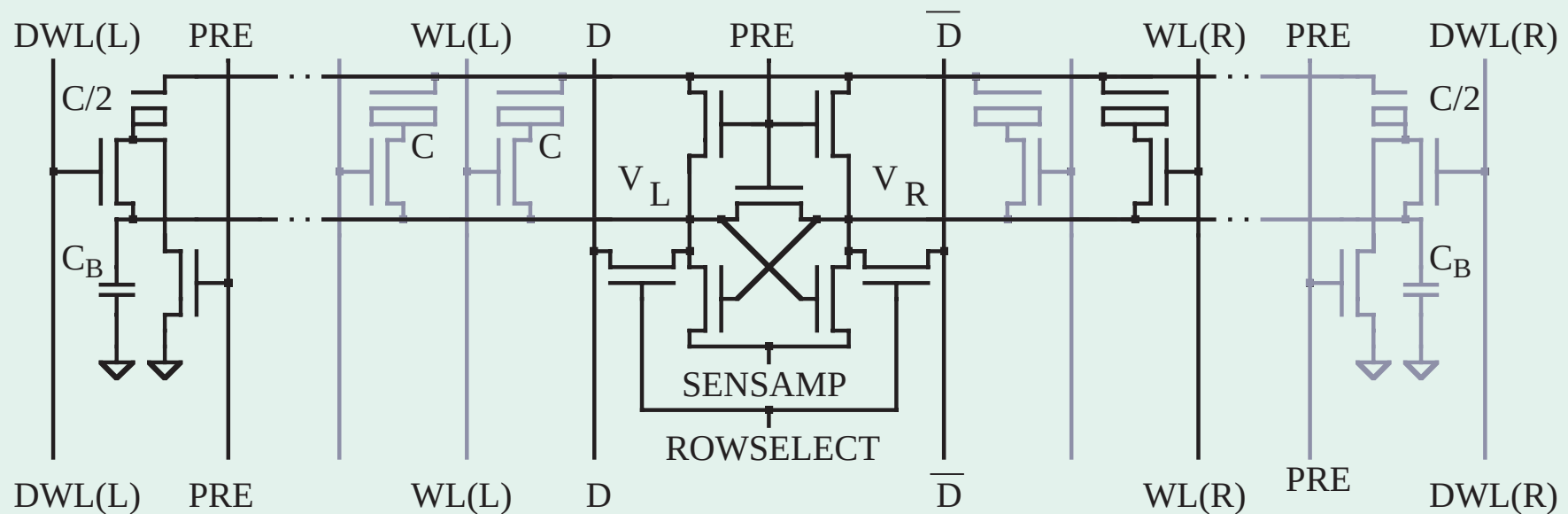
DRAM basics

Memory architecture



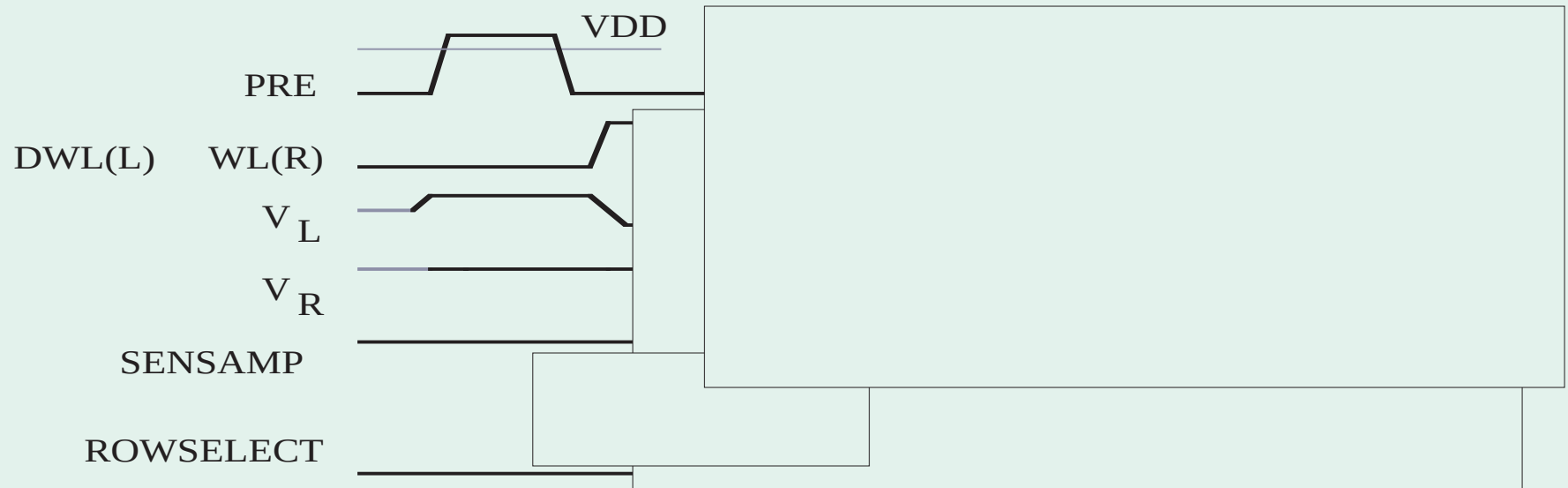
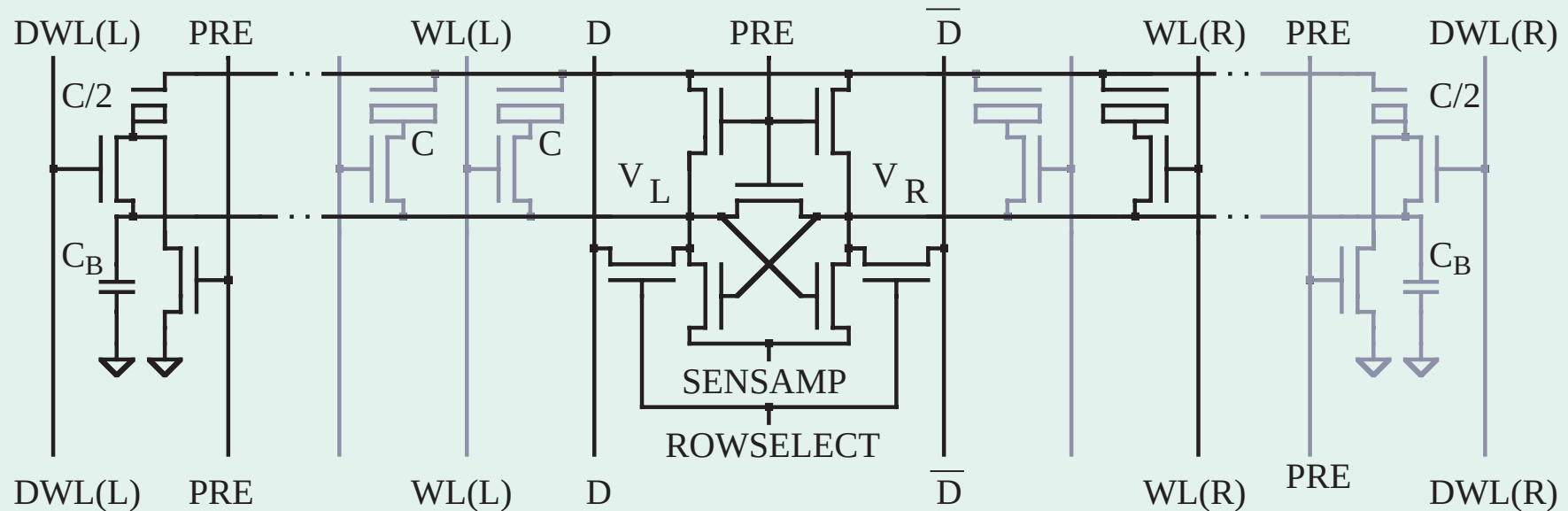
DRAM circuitry

Read/refresh operation



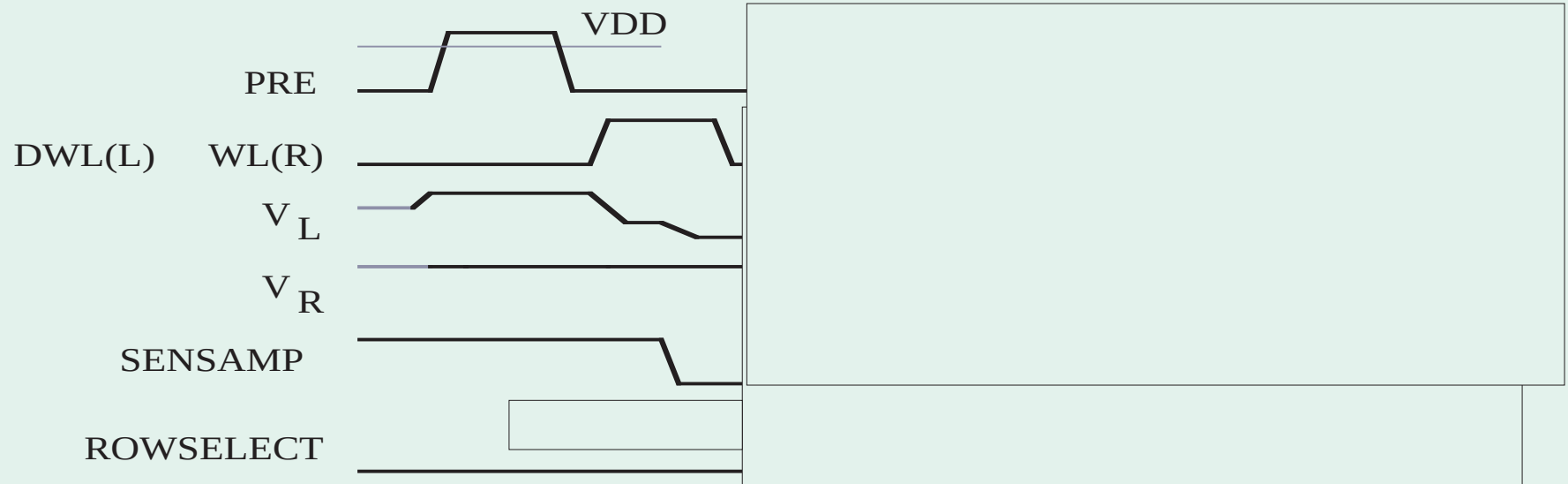
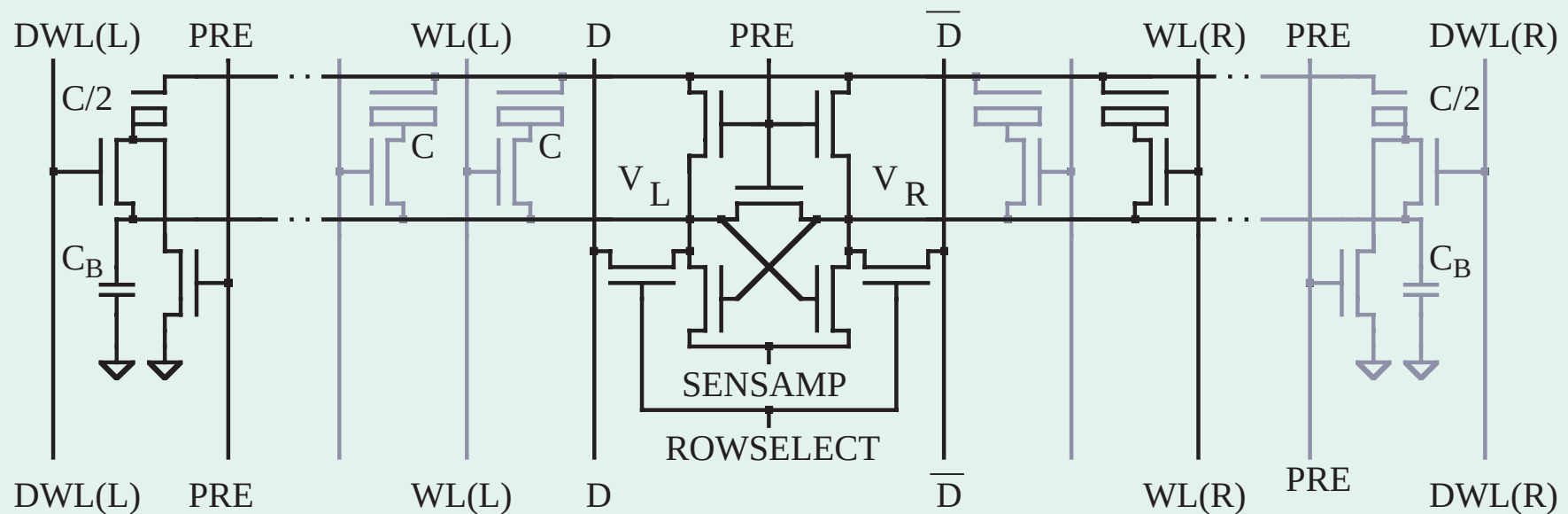
DRAM circuitry

Read/refresh operation



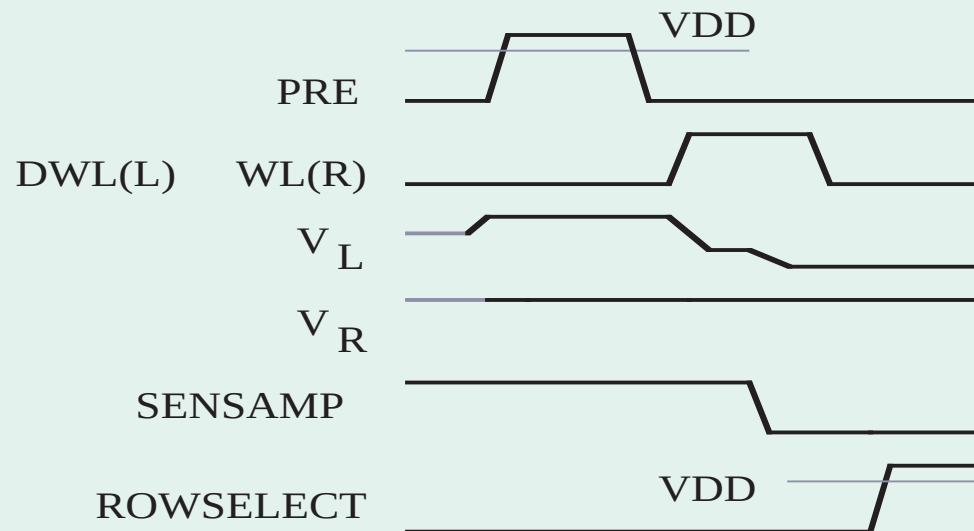
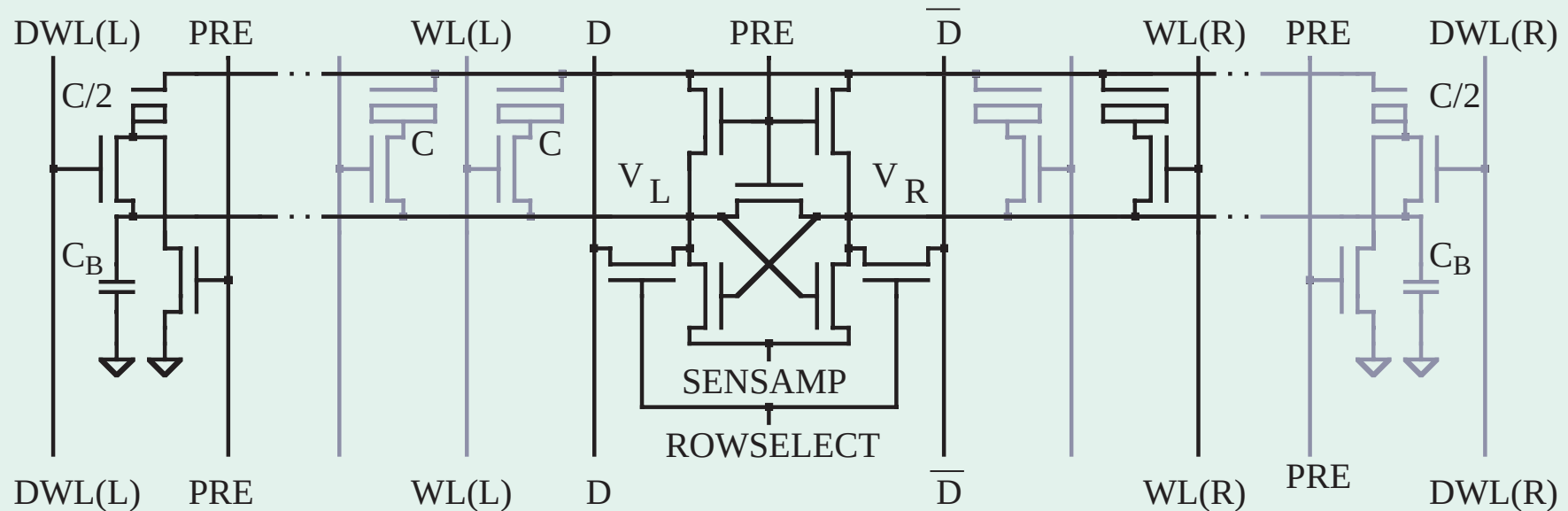
DRAM circuitry

Read/refresh operation



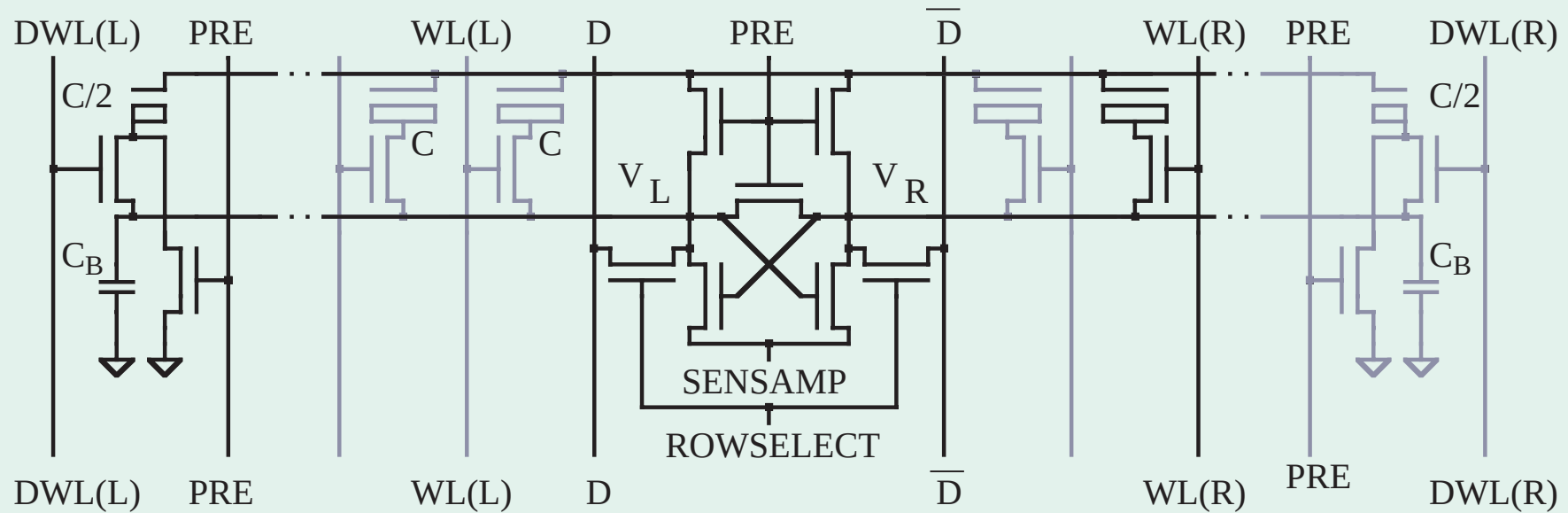
DRAM circuitry

Read/refresh operation

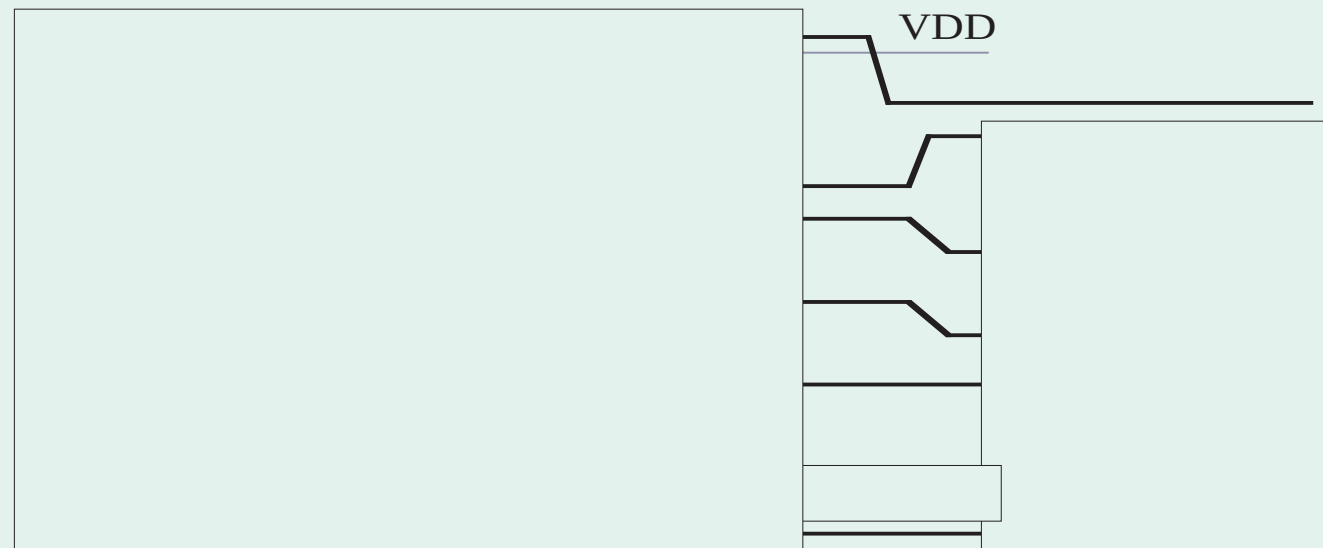


DRAM circuitry

Read/refresh operation

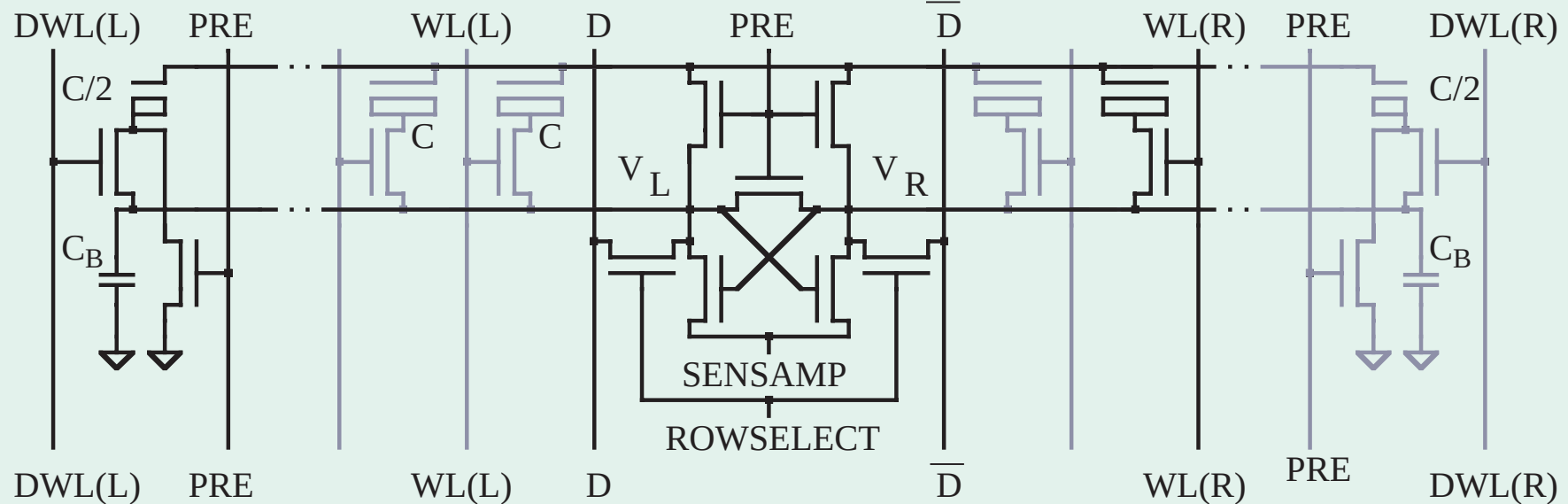


PRE
 $DWL(L)$ $WL(R)$
 V_L
 V_R
 $SENSAMP$
 $ROWSELECT$

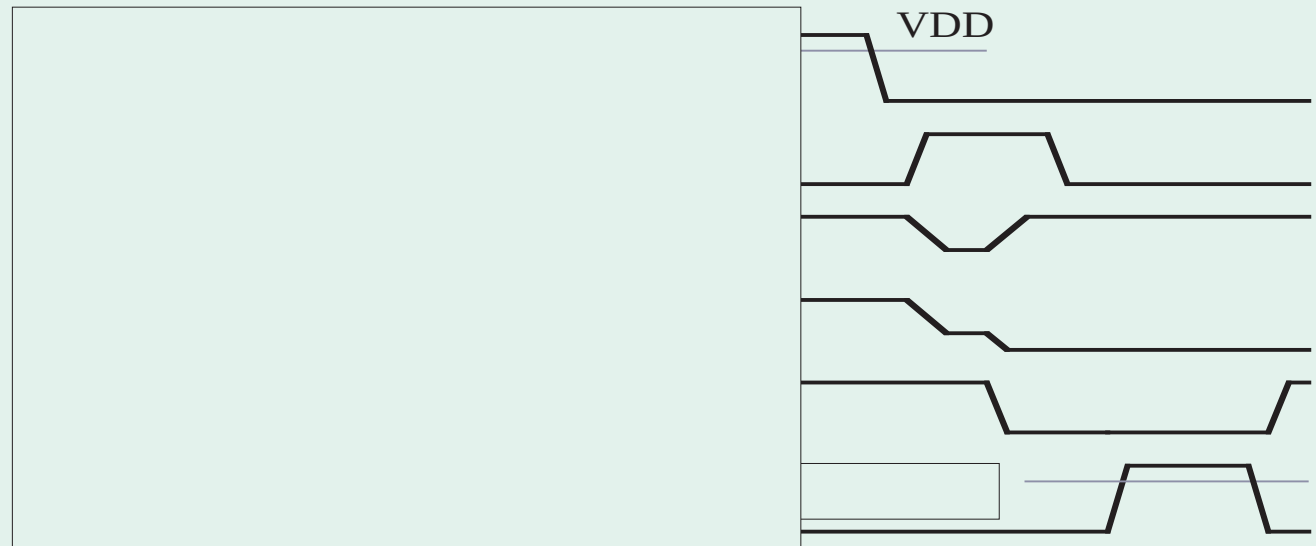


DRAM circuitry

Read/refresh operation

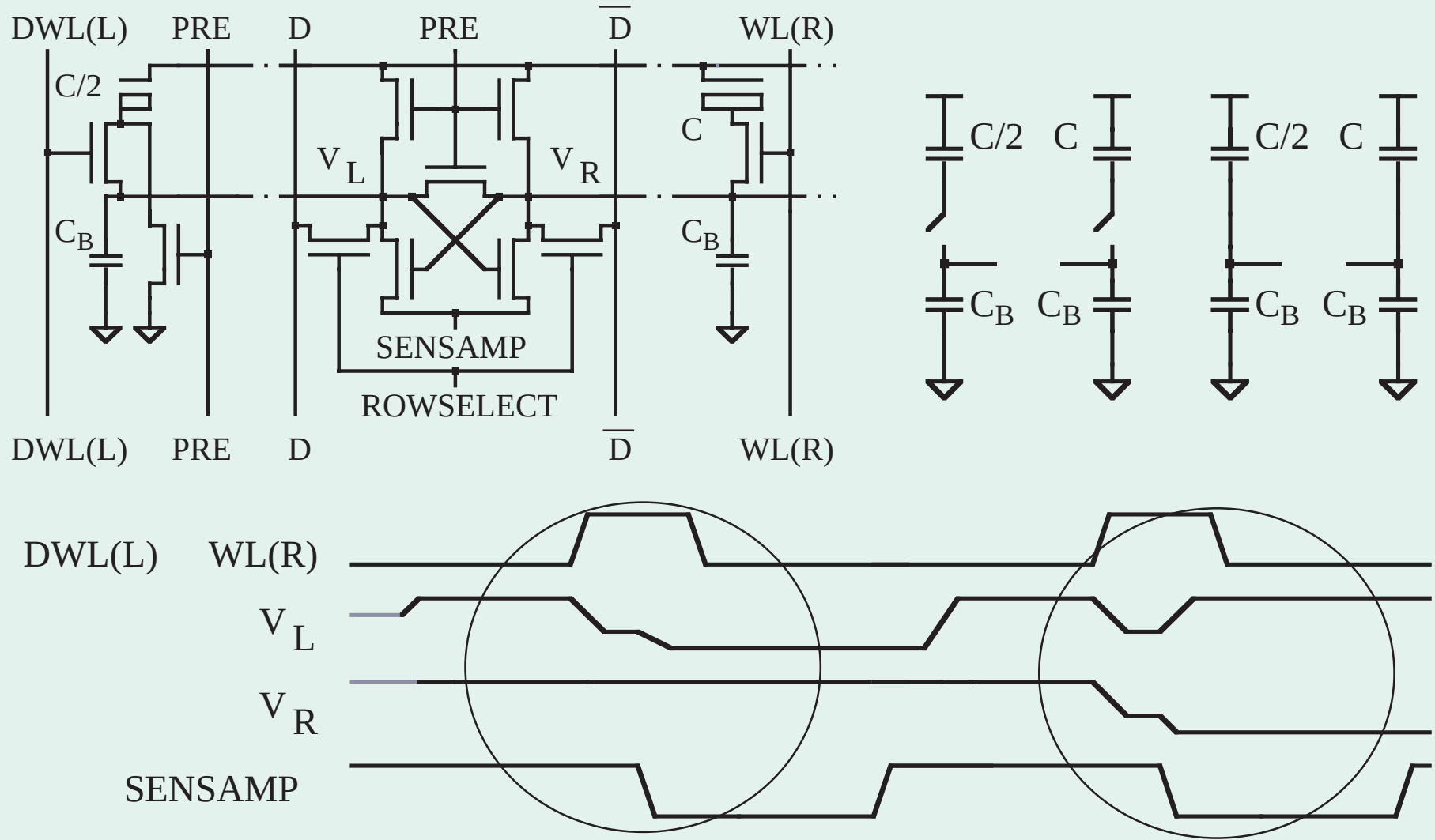


PRE
DWL(L) WL(R)
 V_L
 V_R
SENSAMP
ROWSELECT



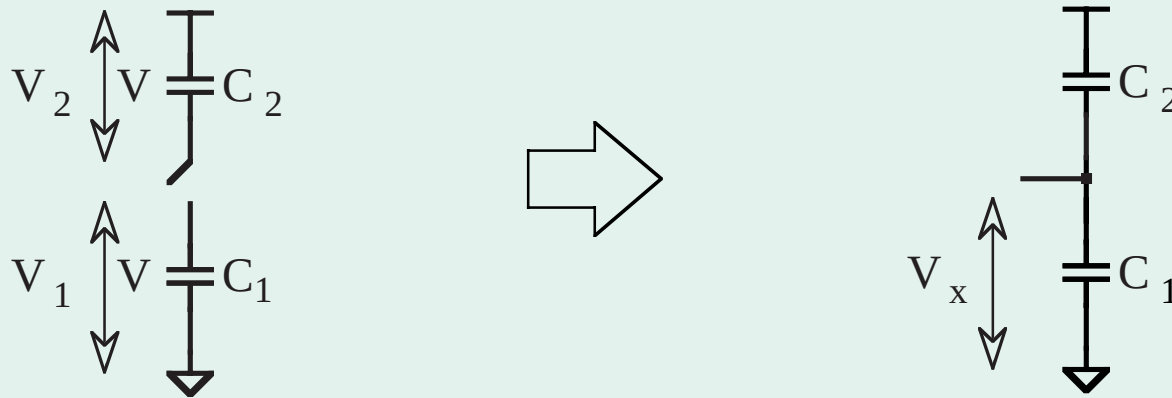
DRAM circuitry

Charge sharing



DRAM circuitry

Charge sharing

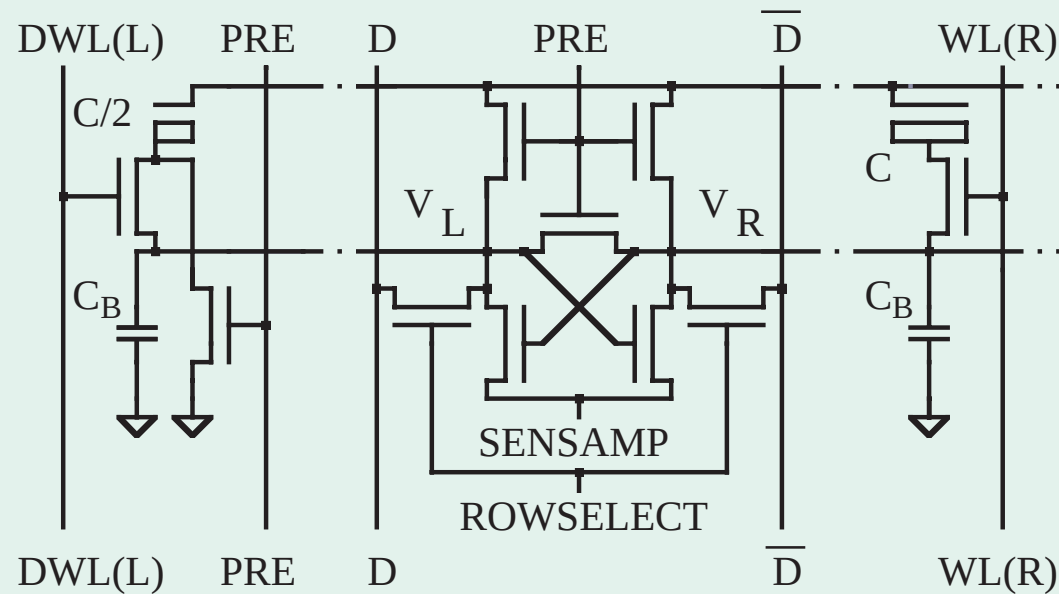


$$V_x = \frac{V_1 C_1 + V_2 C_2}{C_1 + C_2}$$

DRAM circuitry

Charge sharing

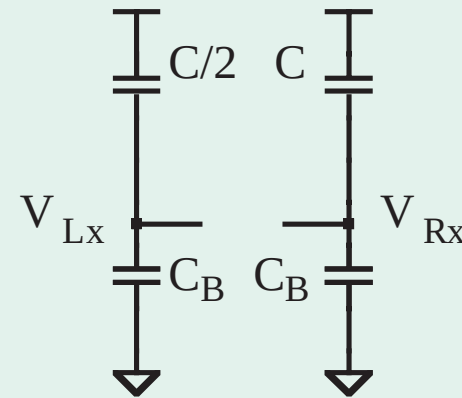
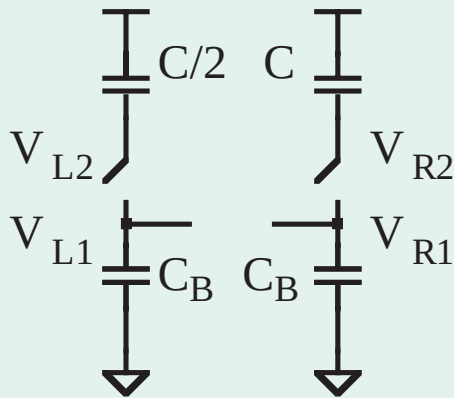
$$V_x = \frac{V_1 C_1 + V_2 C_2}{C_1 + C_2}$$



DRAM circuitry

Charge sharing

$$V_x = \frac{V_1 C_1 + V_2 C_2}{C_1 + C_2}$$



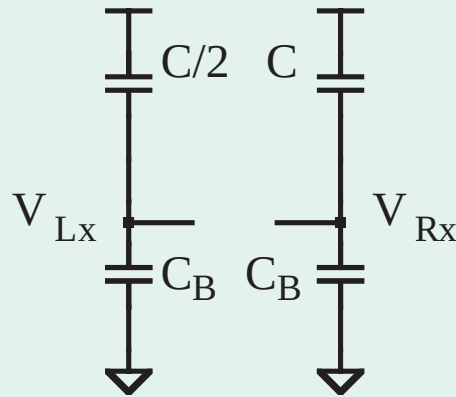
$$V_{Lx} = \frac{V_{DD} C_B}{C_B + C/2}$$

$$V_{Rx} = \frac{V_{DD} C_B}{C_B + C}$$

$$V_{Rx} = \frac{V_{DD} C_B + V_{DD} C}{C_B + C}$$

DRAM circuitry

Charge sharing



$$V_{Lx} = \frac{V_{DD} C_B}{C_B + C/2} > V_{Rx} = \frac{V_{DD} C_B}{C_B + C}$$

$$V_{Lx} = \frac{V_{DD} C_B}{C_B + C/2} < V_{Rx} = V_{DD}$$

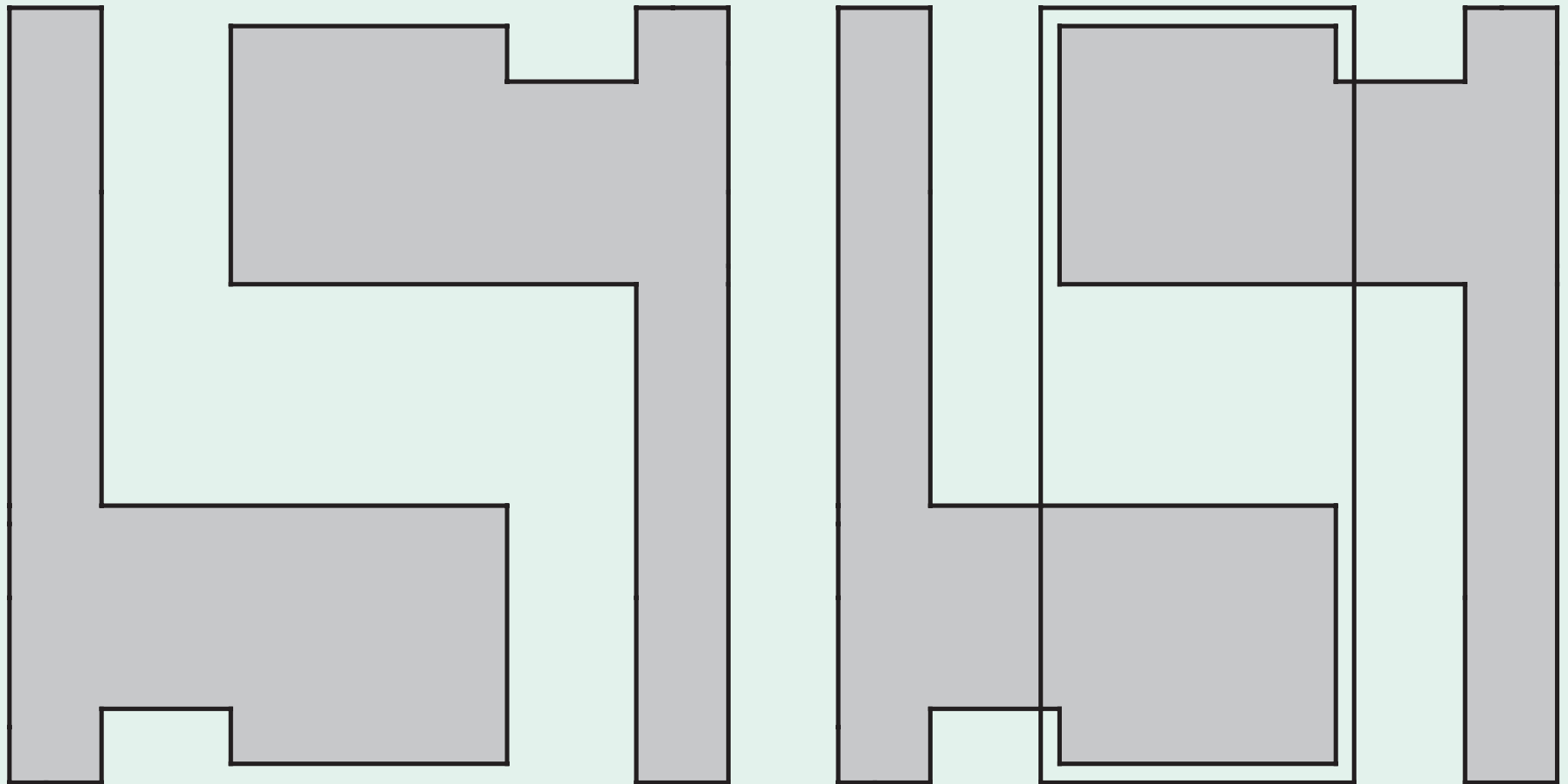
DRAM circuitry

DRAM design trends/limitations

$$V_{LX} = \frac{V_{DD} C_B}{C_B + C/2} > V_{RX} = \frac{V_{DD} C_B}{C_B + C}$$

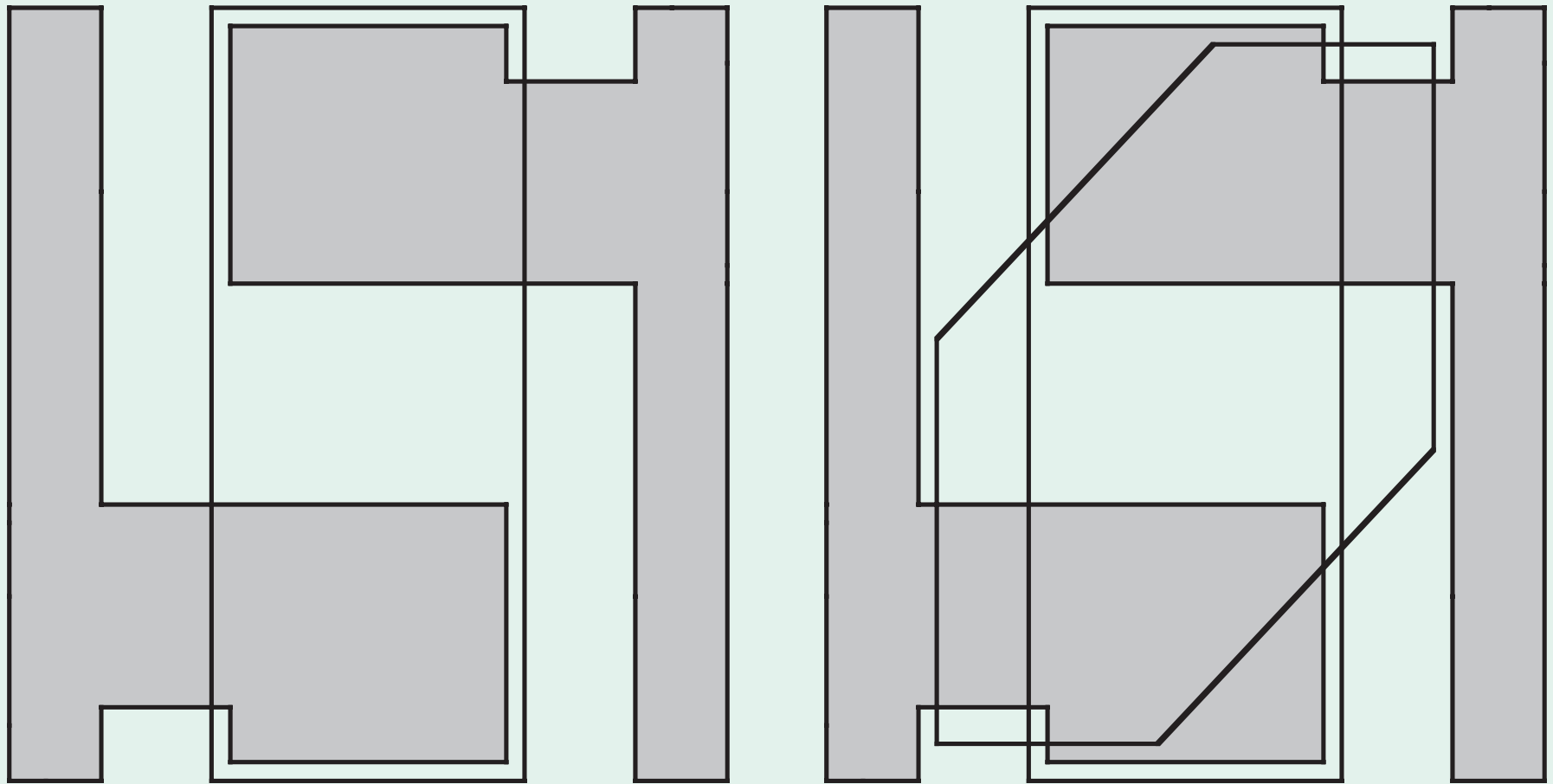
Bit line to cell capacitance high ratio !!!

DRAM layout



Active $\Rightarrow$ Gate oxide $\Rightarrow$ Poly I

DRAM layout



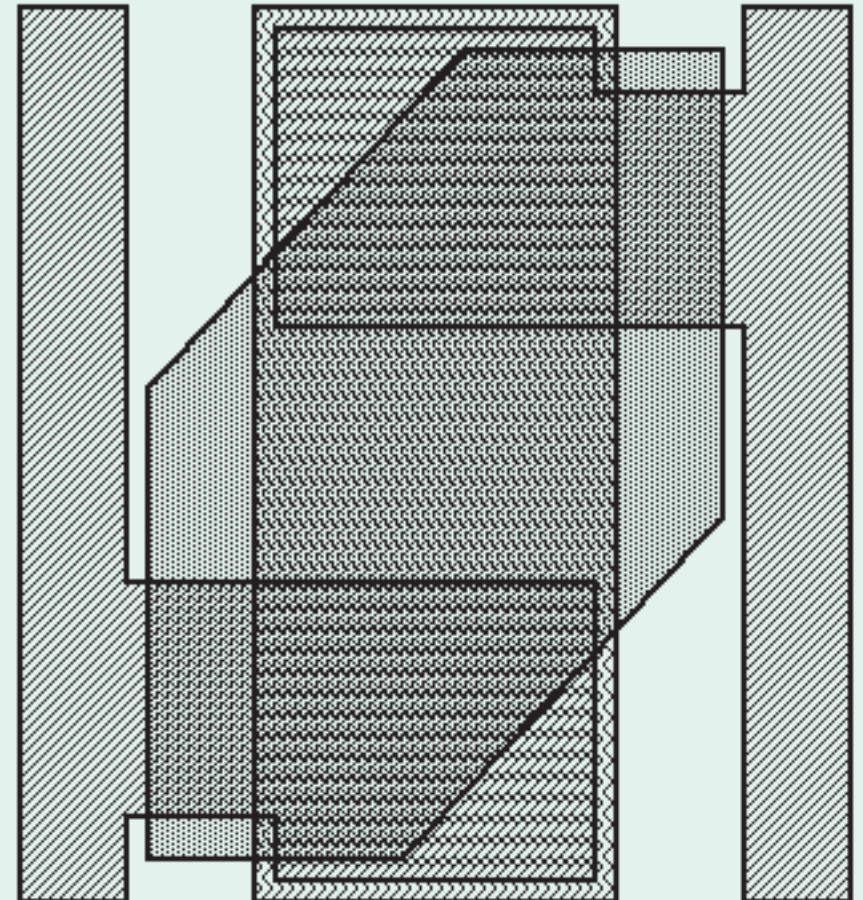
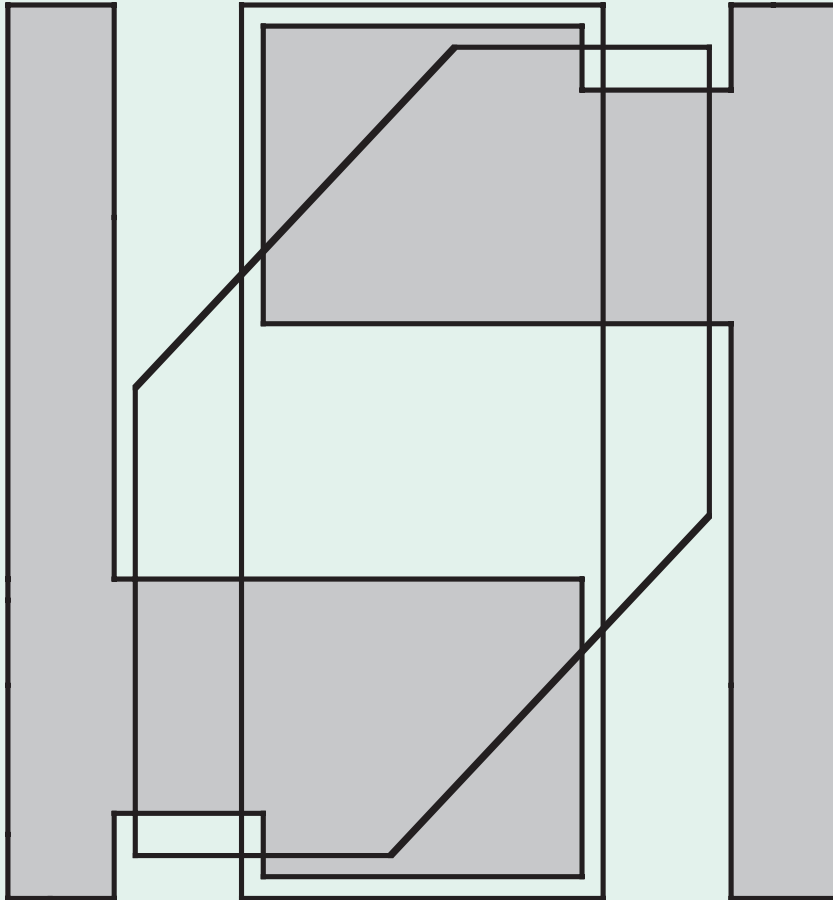
Poly I $\Rightarrow$

Oxide

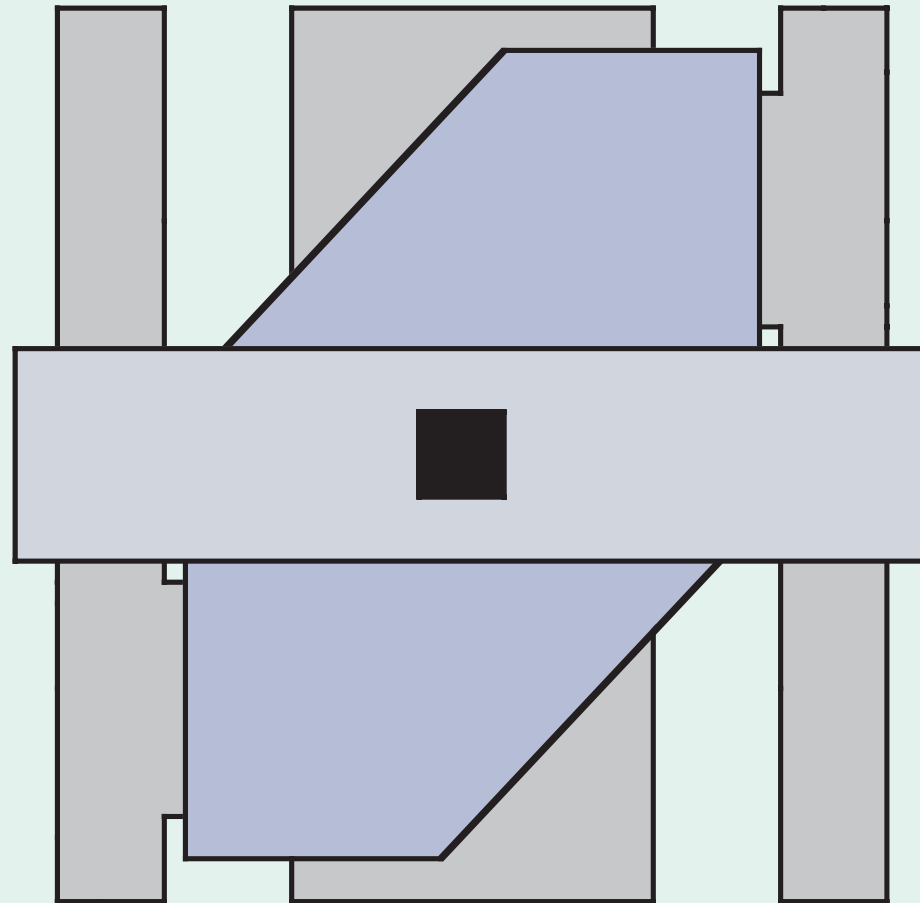
$\Rightarrow$

Poly II

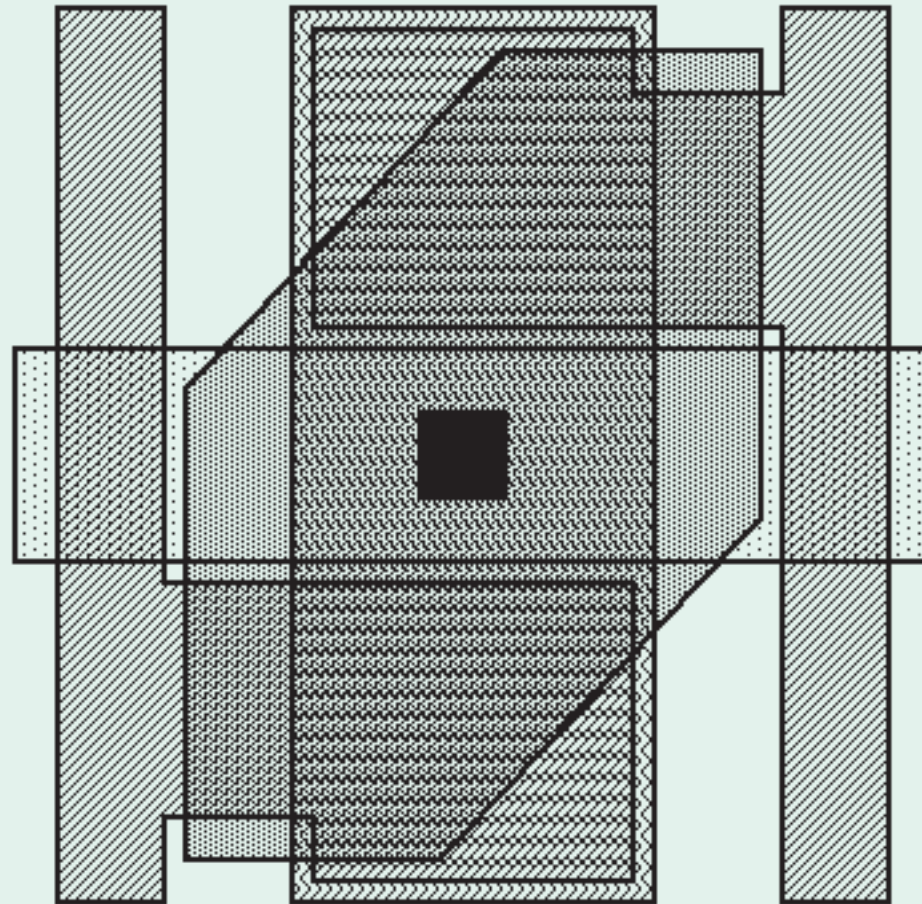
DRAM layout



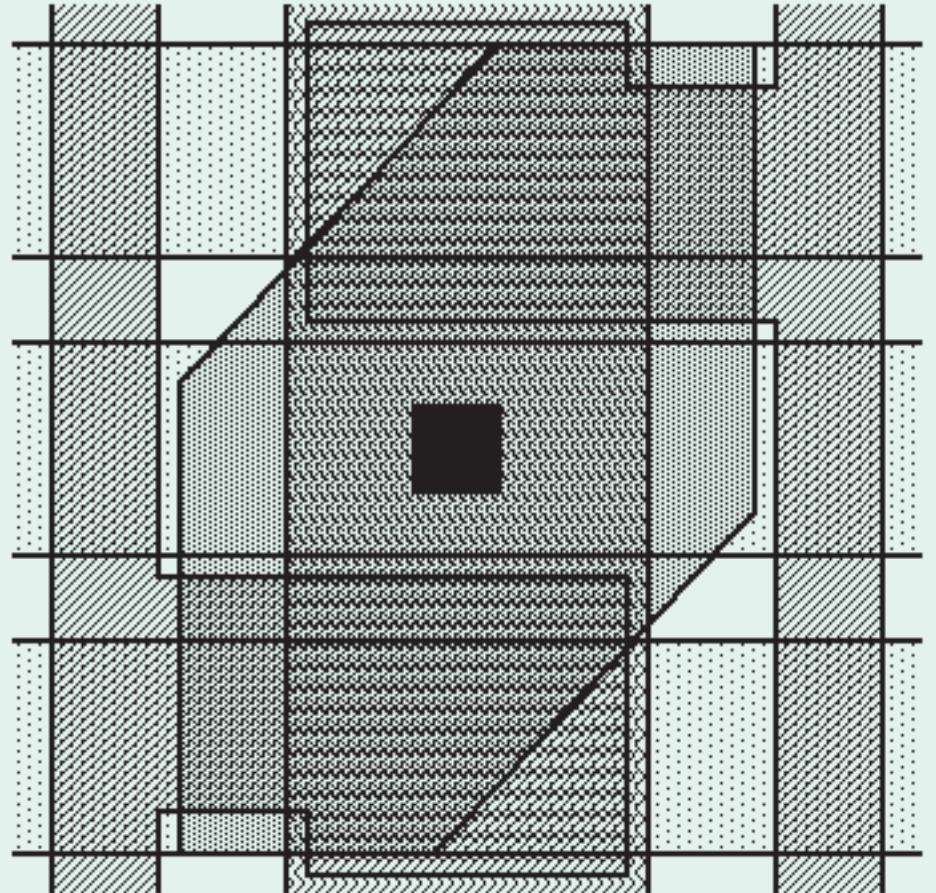
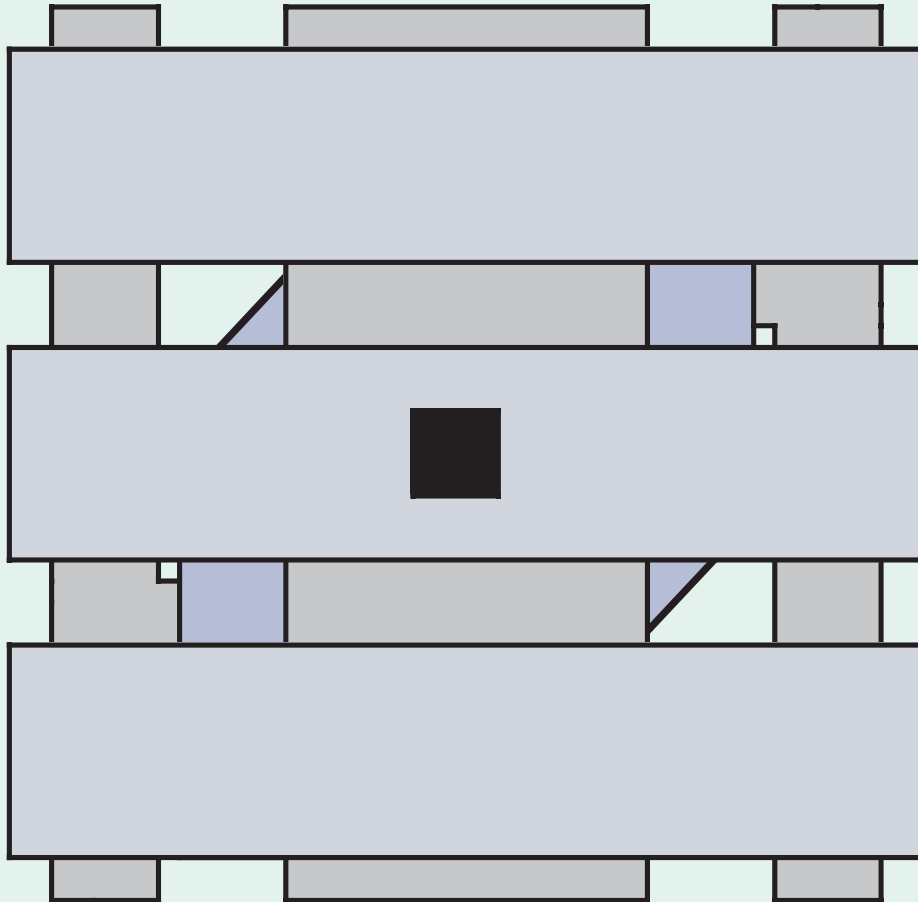
DRAM layout



DRAM layout



DRAM layout



DRAM layout

