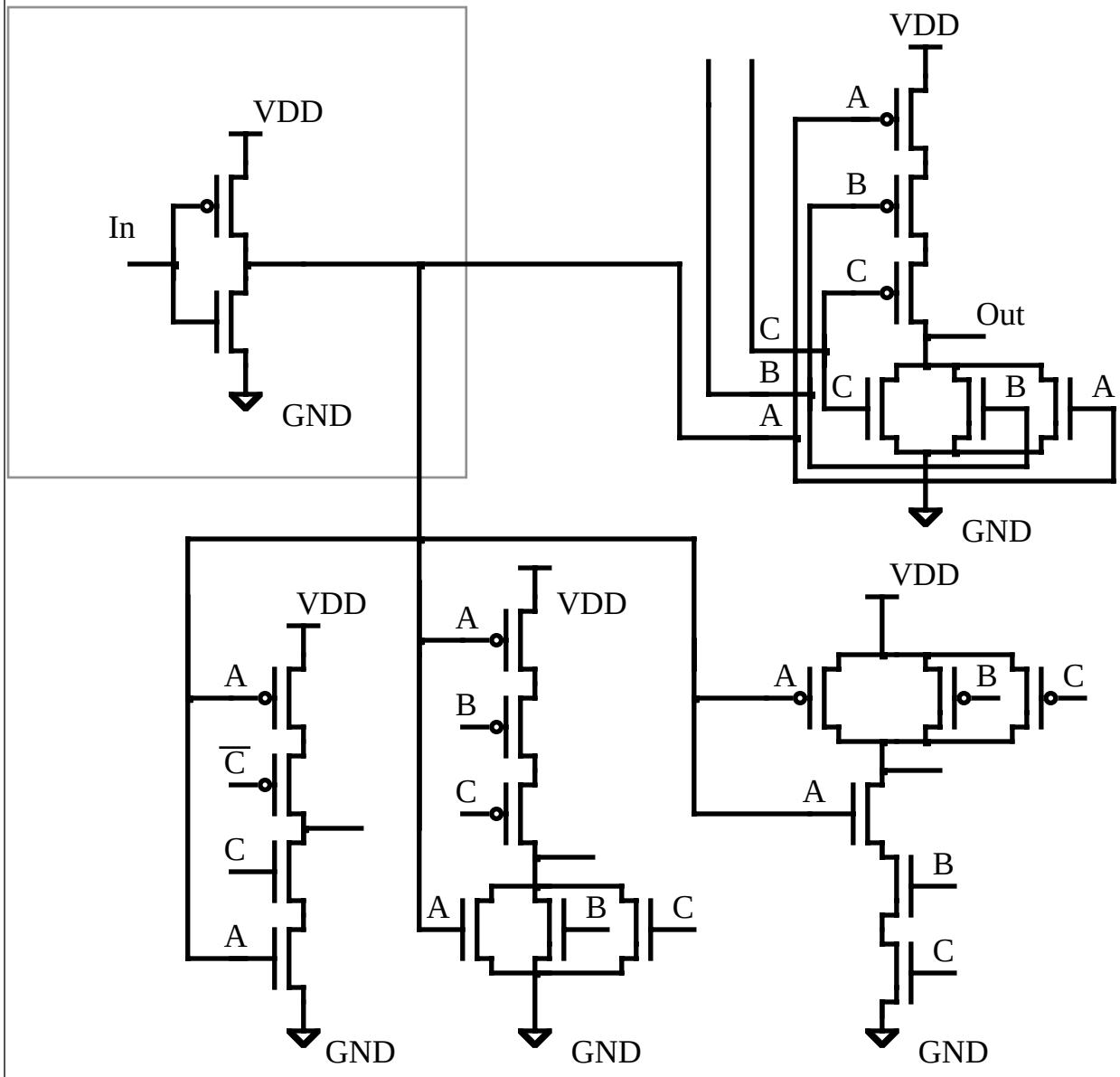
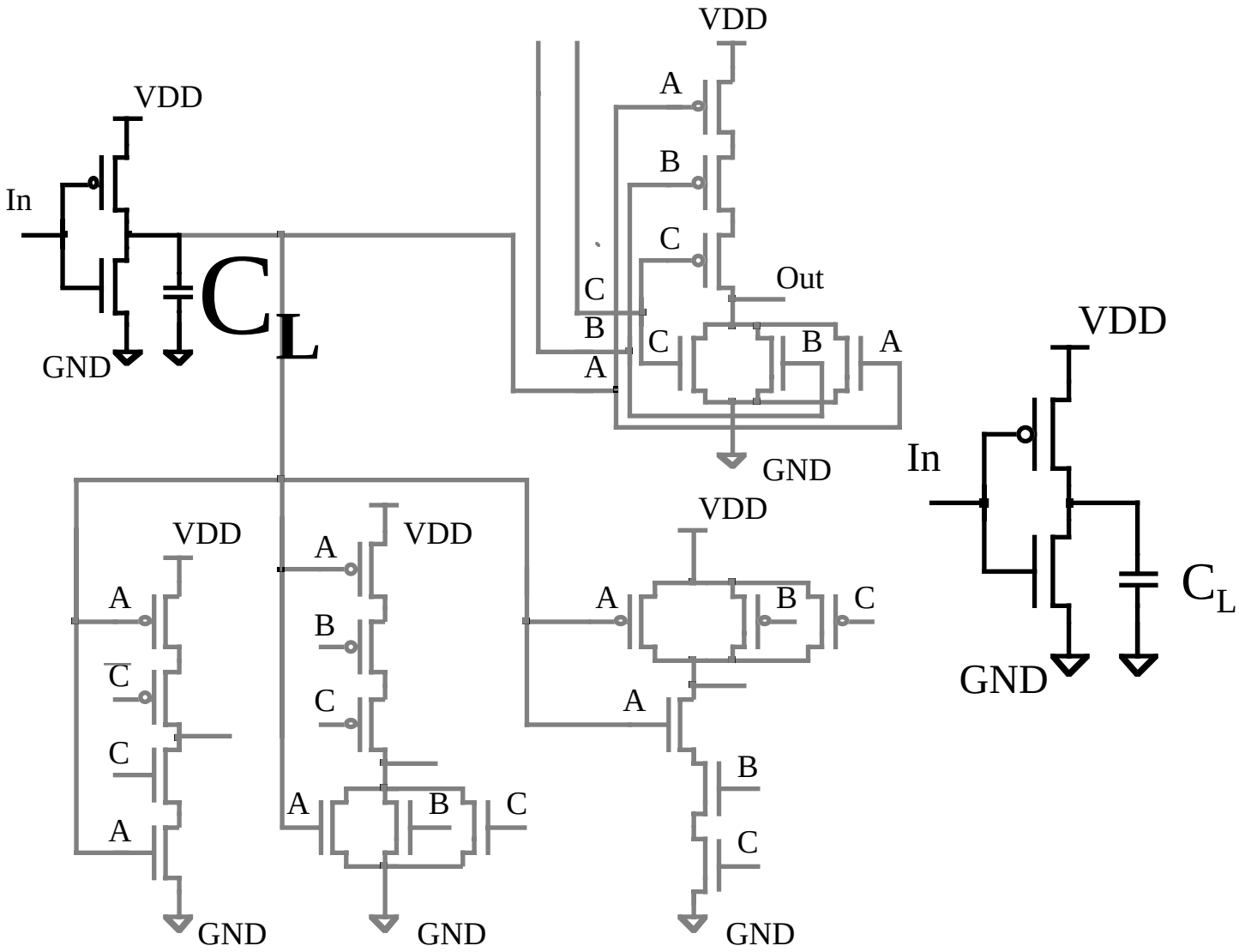
18-322 Lecture 19
CMOS Gates: Sizing and Delay

- Load Capacitance
- Fall and rise time analysis.
- Analytical models.
- Propagation delay analysis.
- Fall and rise time formulas
- Transistor sizing
- Multi-input gates

Text: Sections 3.3.3 and 4.2

CMOS Inverter's Load




VDD
In
GND
C_L
VDD
A
B
C
Out
C
B
A
C
B
A
GND
VDD
In
C_L
GND
VDD
A
B
C
C
C
A
GND
VDD
A
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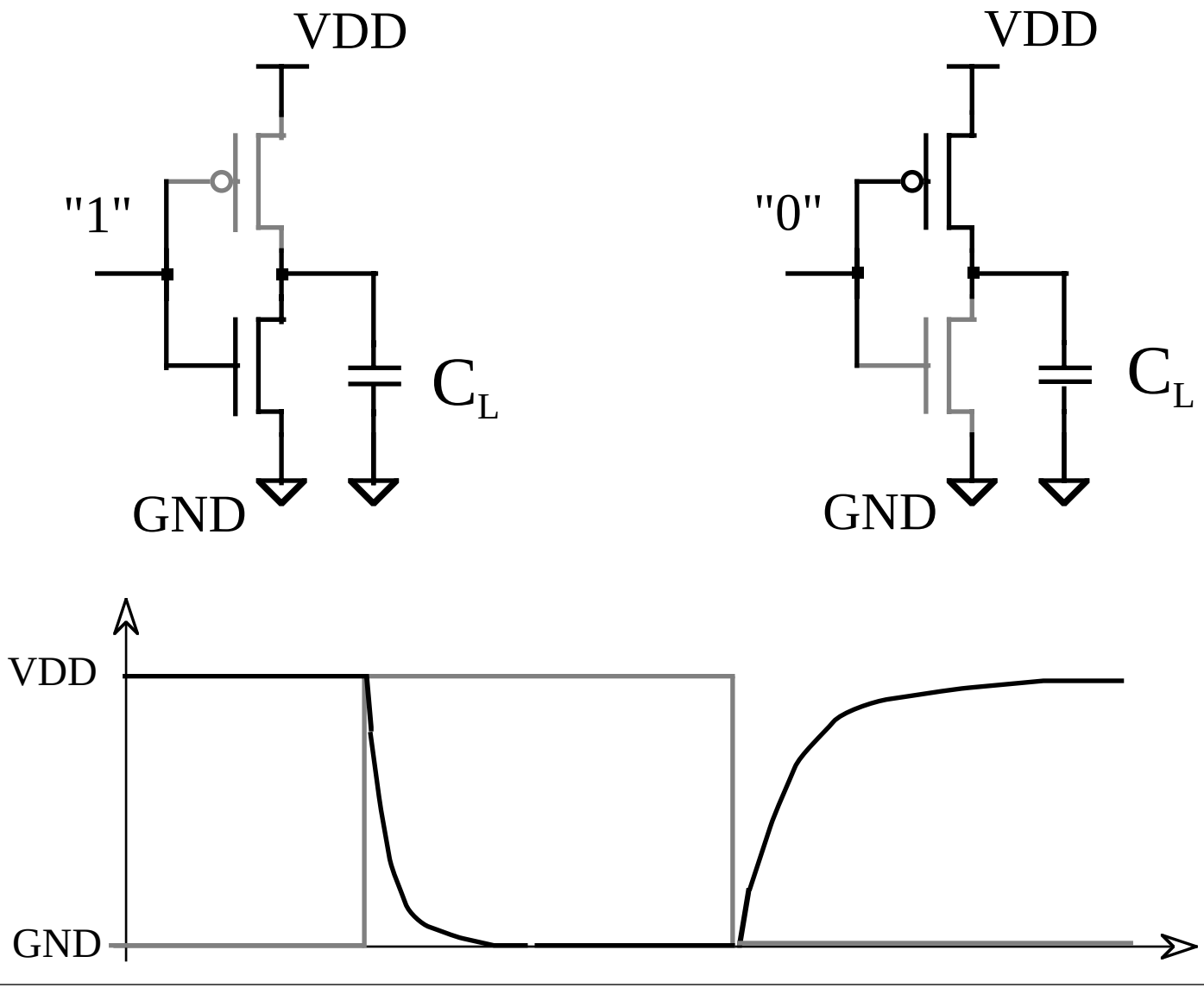
GND
VDD
A
B
C
A
B
C
A
GND

CMOS Inverter - Switching



Device equations (NMOS)

Non-Sat:

$$I_{ds} = \beta_n \left[(V_{gs} - V_{tn}) V_{ds} - \frac{1}{2} V_{ds}^2 \right]$$

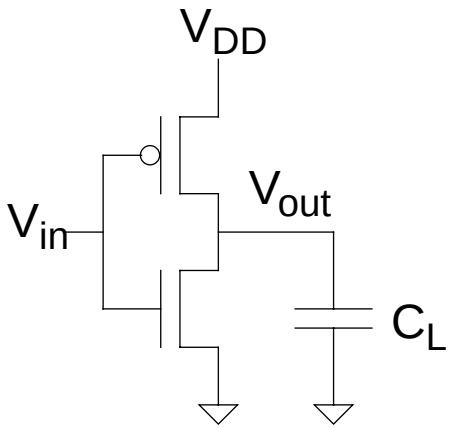
Saturation:

$$I_{ds} = \frac{\beta_n}{2} (V_{gs} - V_{tn})^2$$

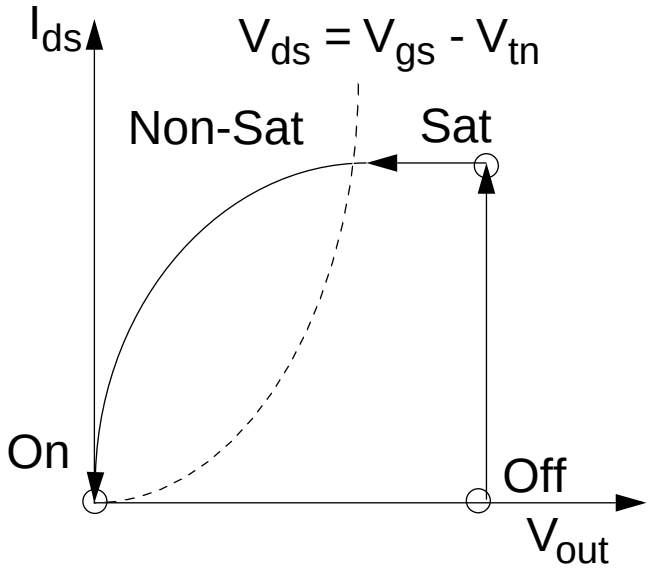
where

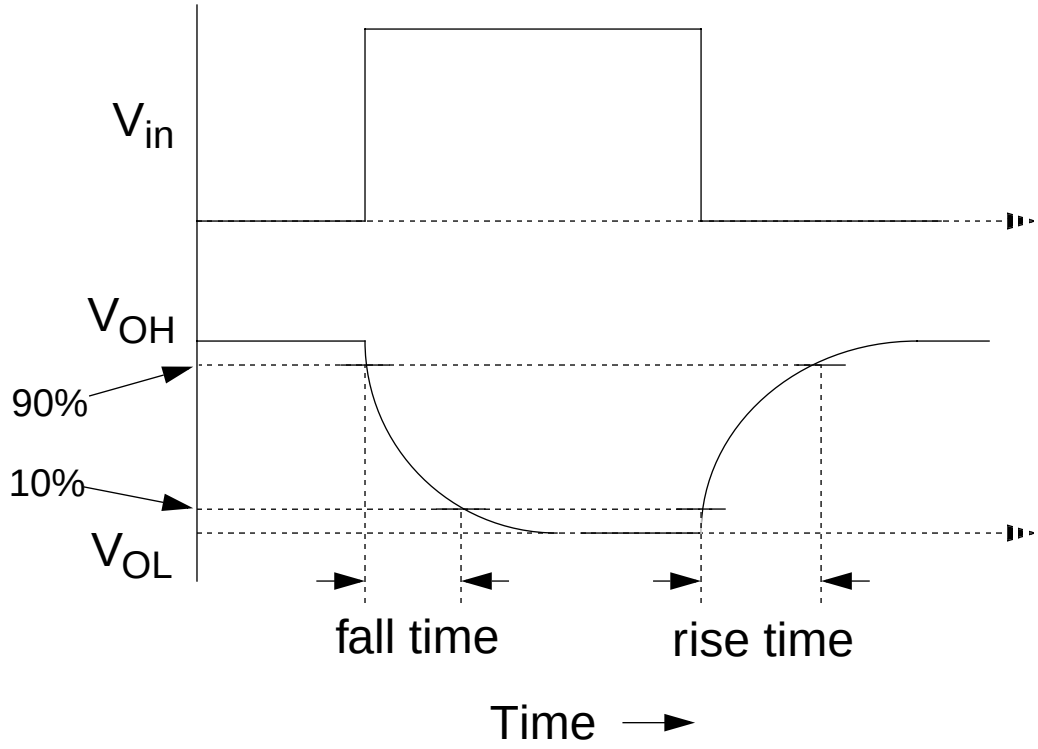
$$\beta_n = \mu \frac{\varepsilon}{t_{ox}} \left(\frac{W}{L} \right)_n$$

Inverter Switching

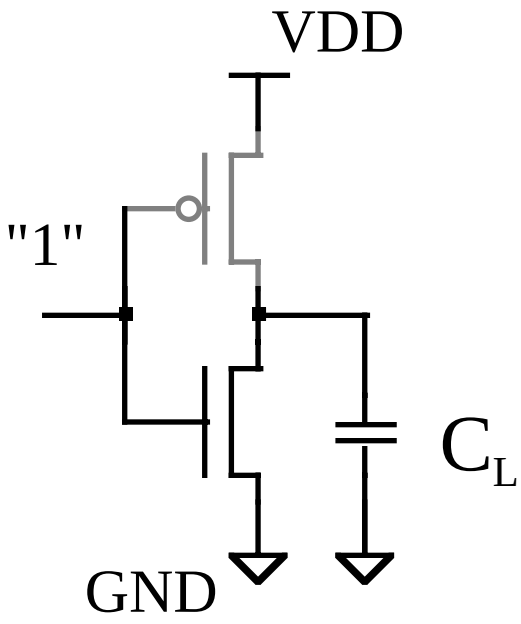


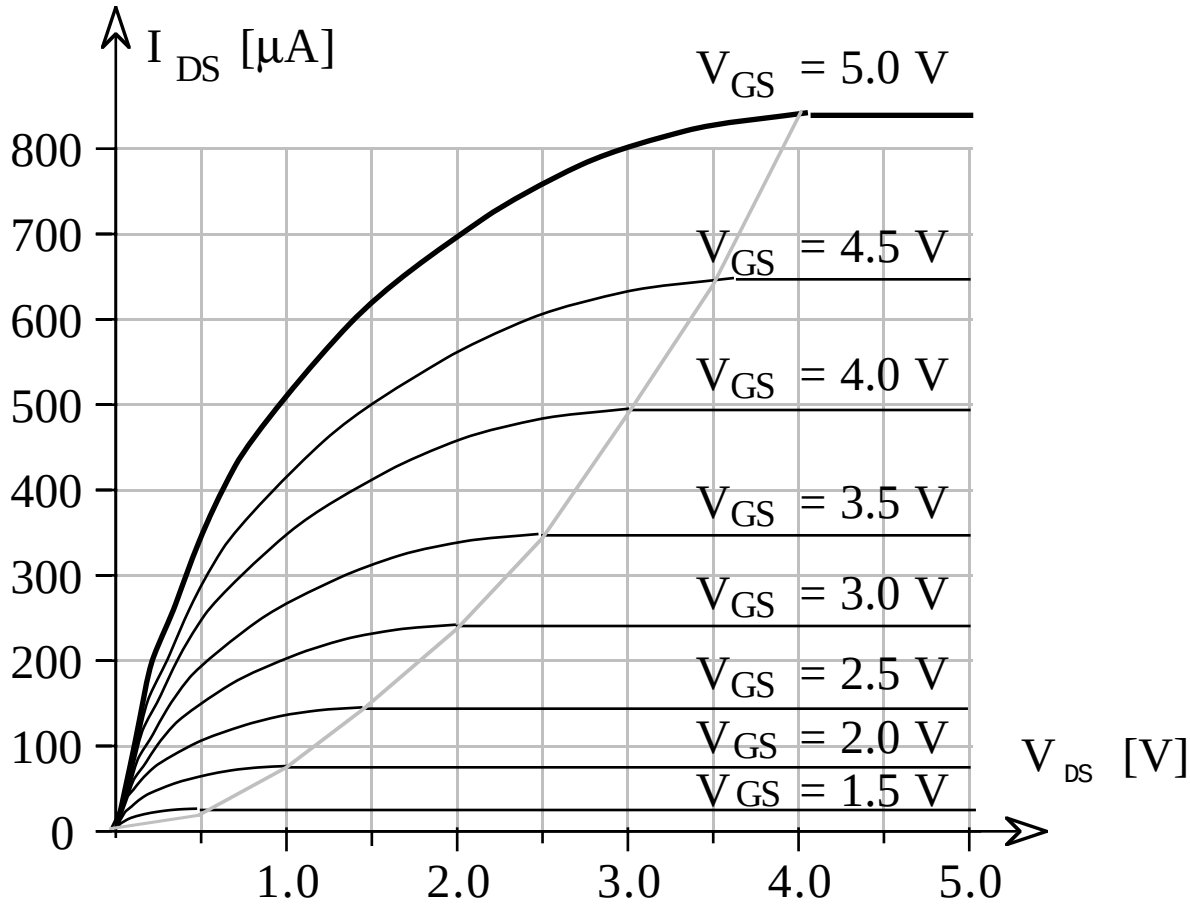
NMOS trajectory: V_{out} falling.



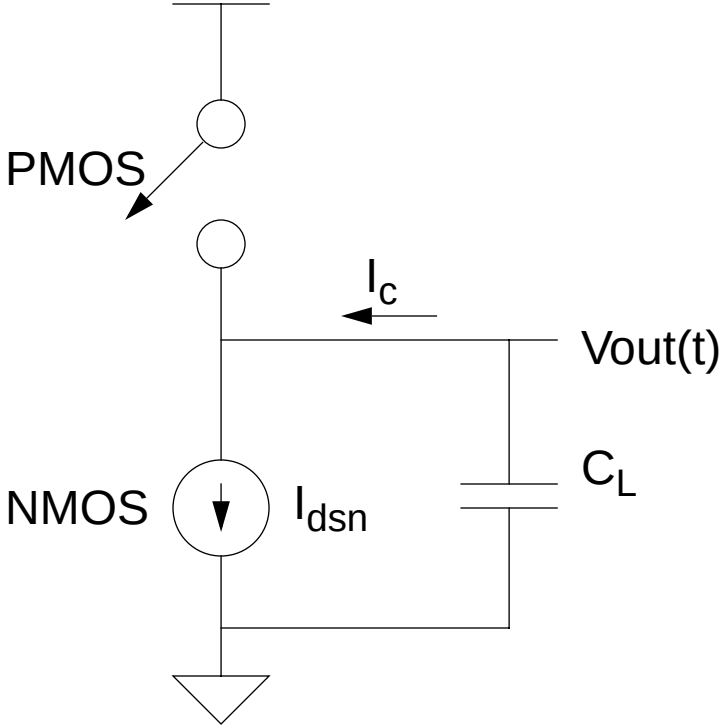


CMOS Inverter - Switching

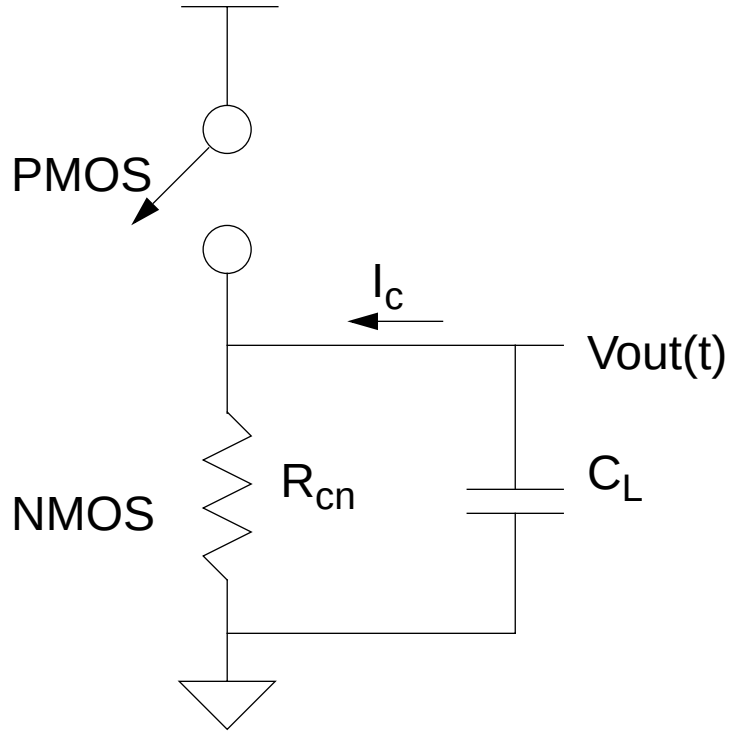




Output Fall Time Analysis



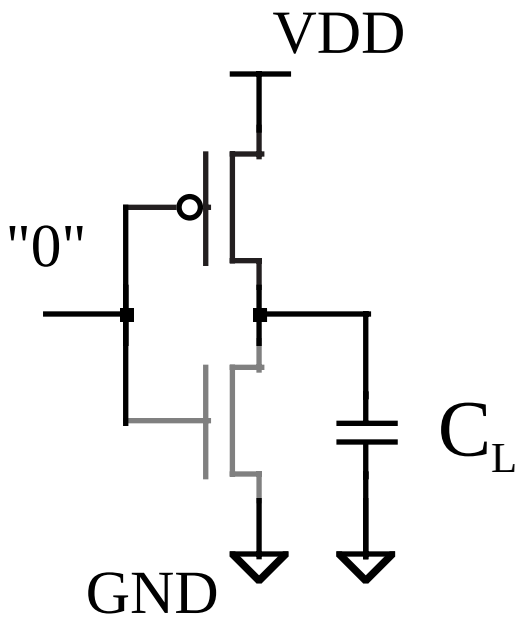
NMOS saturated: $V_{out} \geq V_{DD} - V_{tn}$

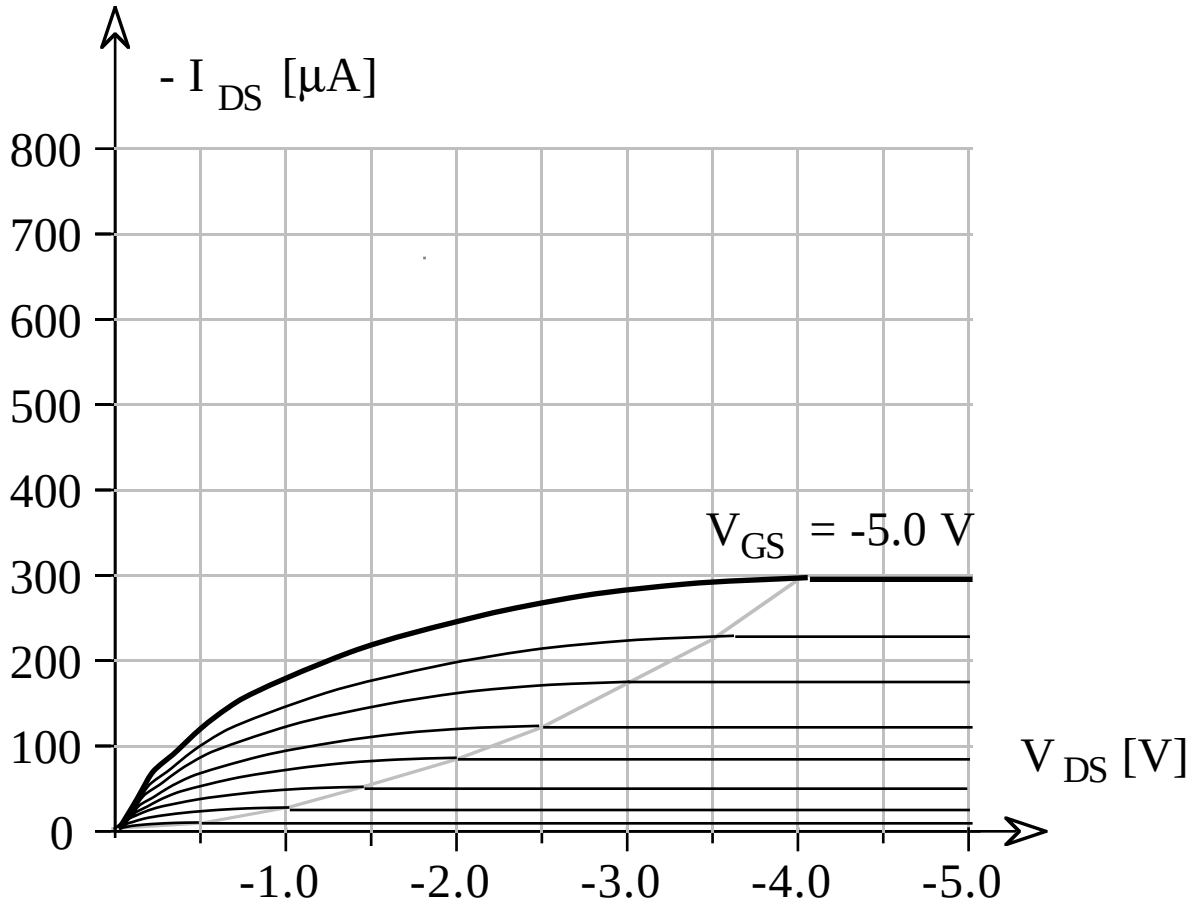


NMOS non-saturated: $0 < V_{out} \leq V_{DD} - V_{tn}$

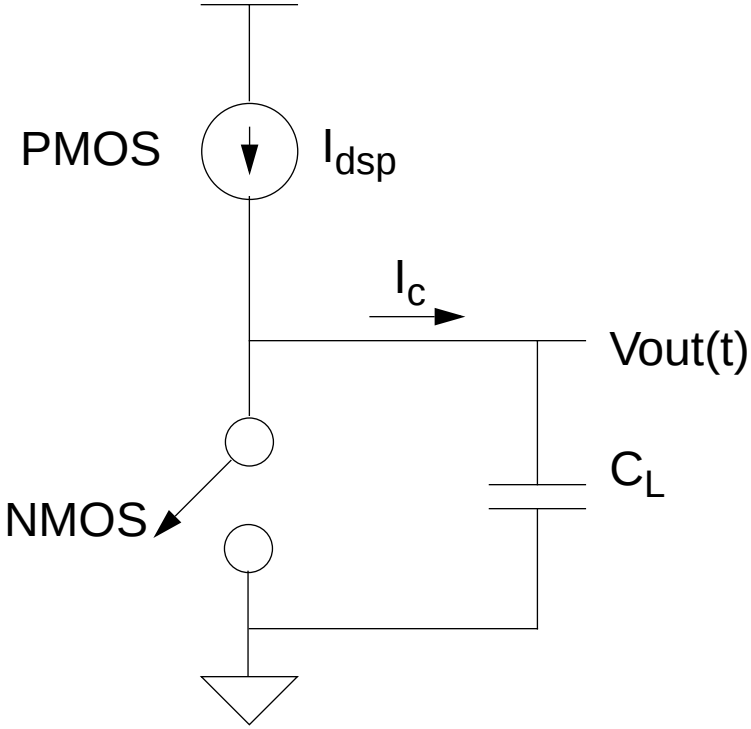
$$t_f = k\frac{C_L}{\beta_n V_{DD}}$$

CMOS Inverter - Switching

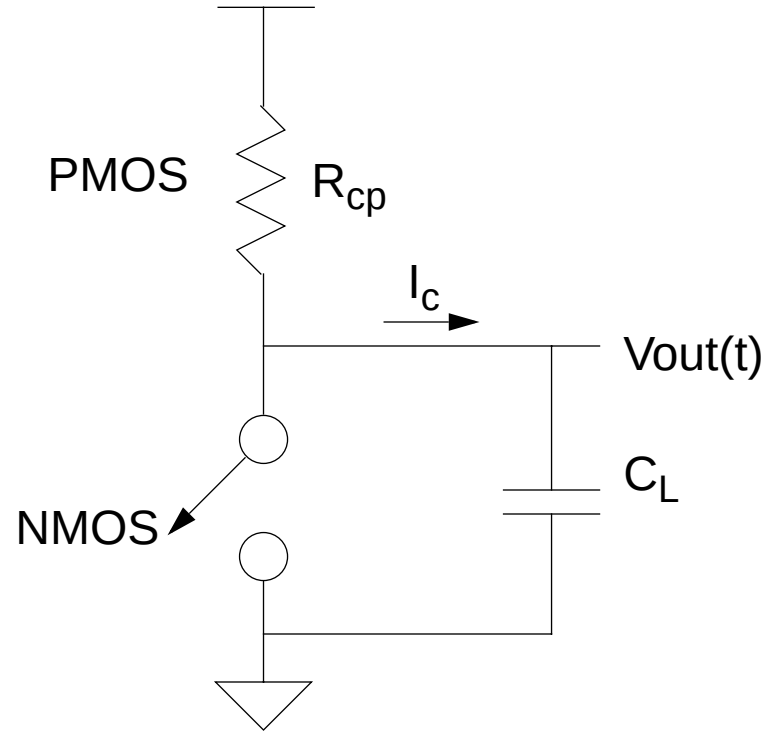




Output Rise Time Analysis



PMOS saturated: $V_{out} \leq |V_{tp}|$



PMOS non-saturated: $|V_{tp}| < V_{out} < V_{DD}$

$$t_r = k\frac{C_L}{\beta_p V_{DD}}$$

Inverter Rise/Fall Time Equalization

- Fall, Rise times:

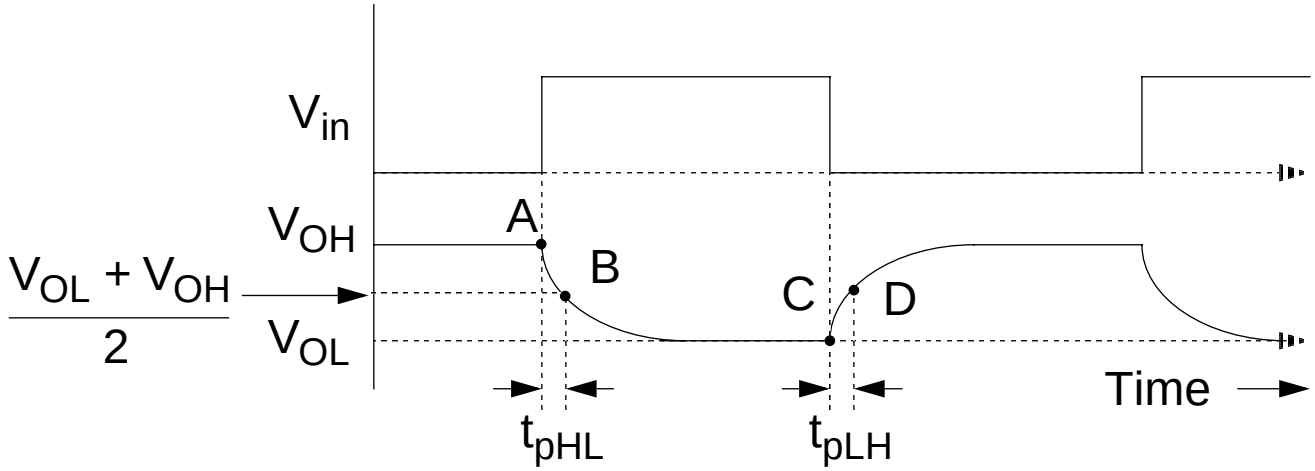
$$\left(t_f = k\frac{C_L}{k_n\left(\frac{W}{L}\right)_n V_{DD}} \right), \left(t_r = k\frac{C_L}{k_p\left(\frac{W}{L}\right)_p V_{DD}} \right)$$

- To equalize rise, fall times:

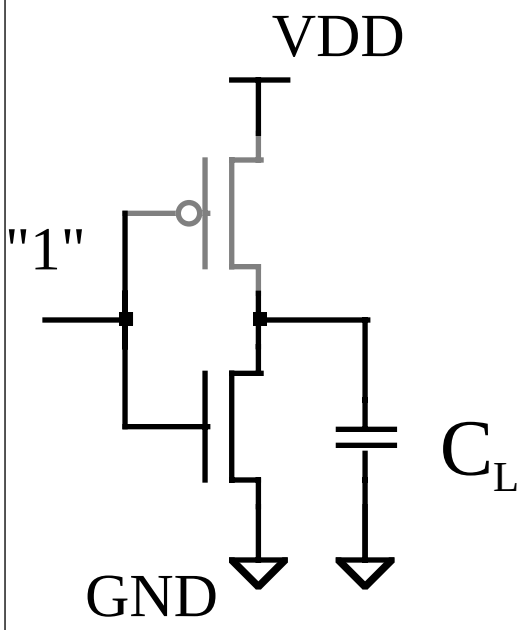
$$(\mu_n = 2\mu_p) \Rightarrow \left(\left(\frac{W}{L}\right)_p \approx 2\left(\frac{W}{L}\right)_n \right)$$

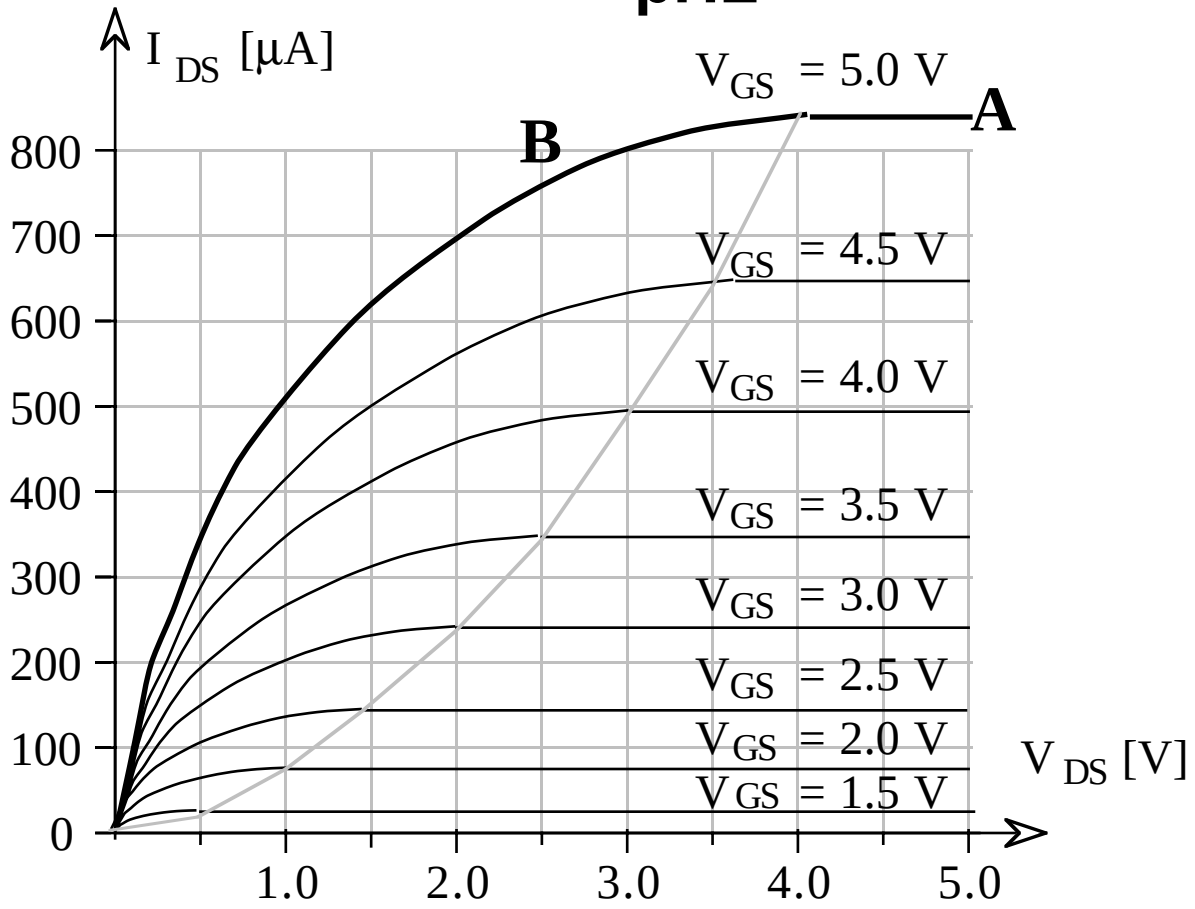
Propagation Delays

- $\Delta t = \frac{\Delta Q}{I_{avg}} = C_L \frac{\Delta V}{I_{avg}}$.



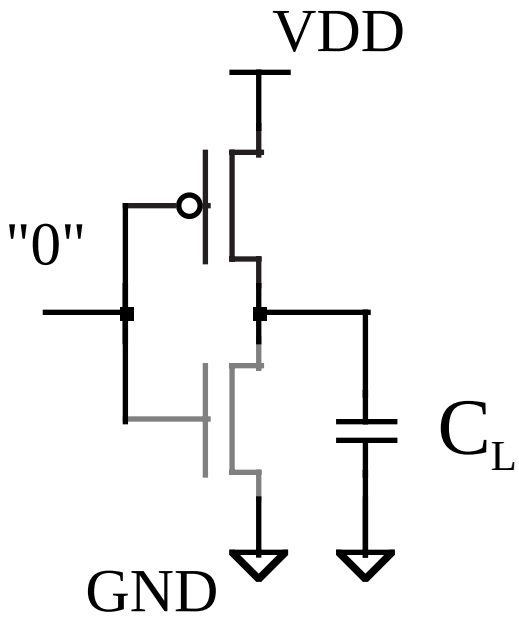
Propagation delay - t_{pHL}

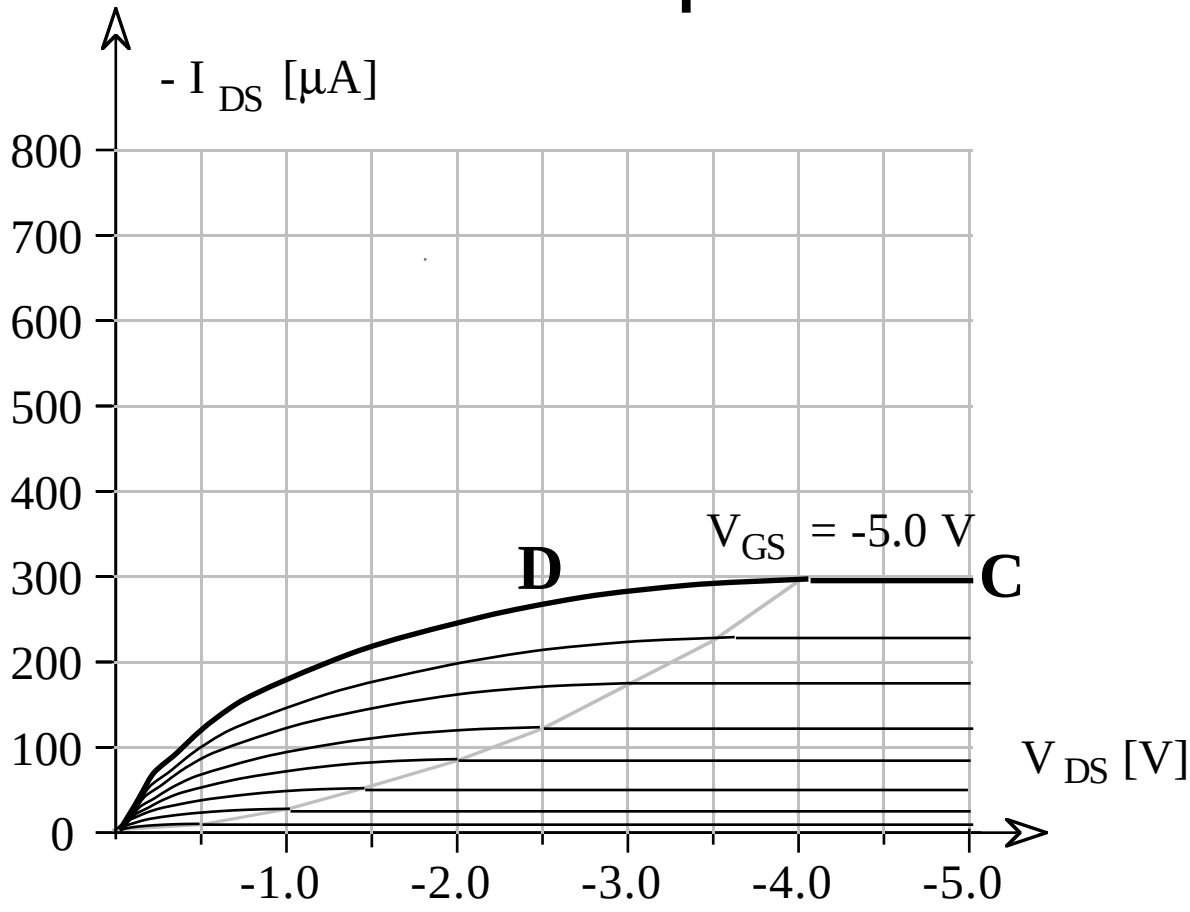




- $t_{pHL} = C_L \dfrac{\frac{1}{2}(V_{OH} - V_{OL})}{I_{avg}}$, $I_{avg} = \dfrac{I_A + I_B}{2}$.

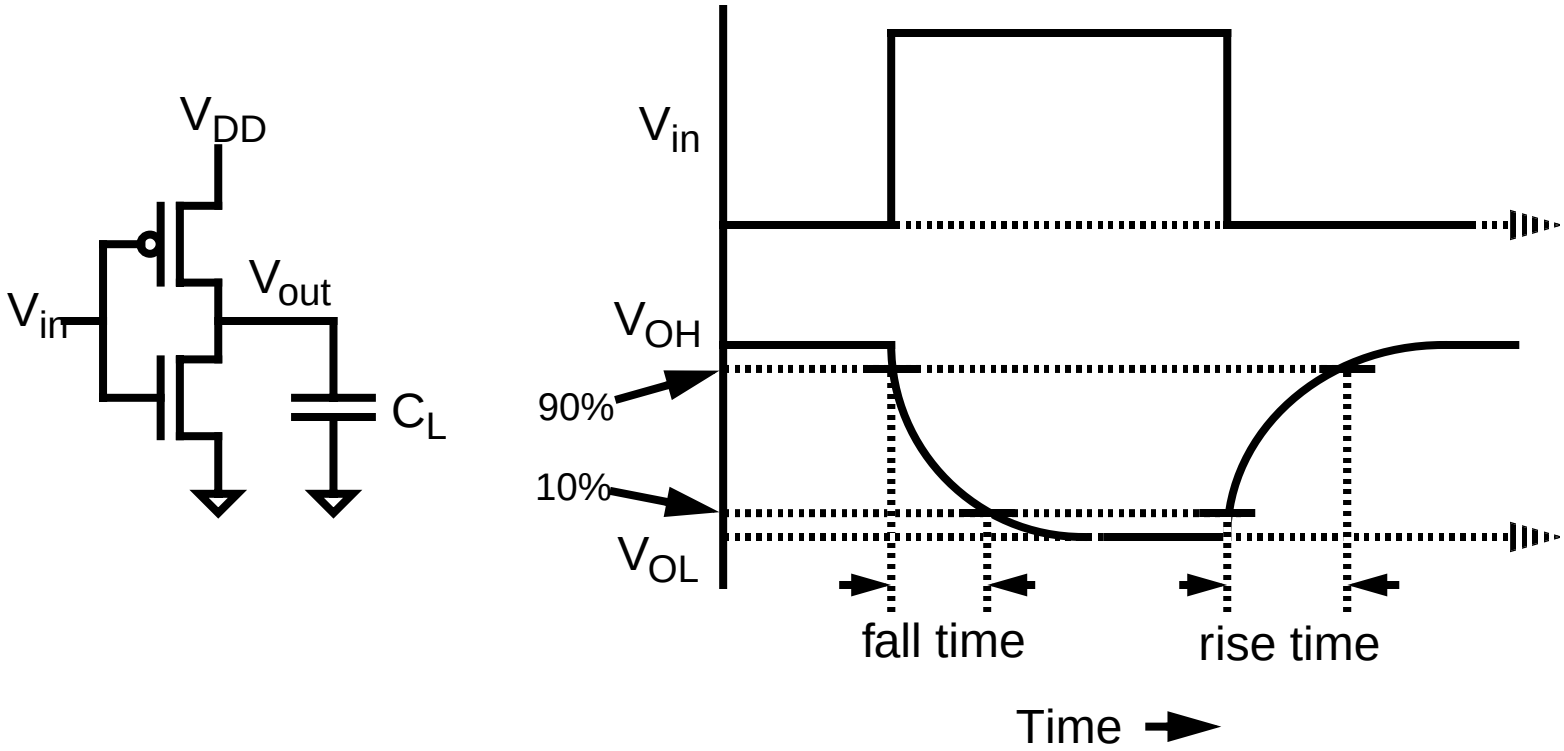
Propagation delay - t_{pLH}





- $t_{pLH} = C_L \dfrac{\frac{1}{2}(V_{OH} - V_{OL})}{I_{avg}}$, $I_{avg} = \dfrac{I_C + I_D}{2}$.

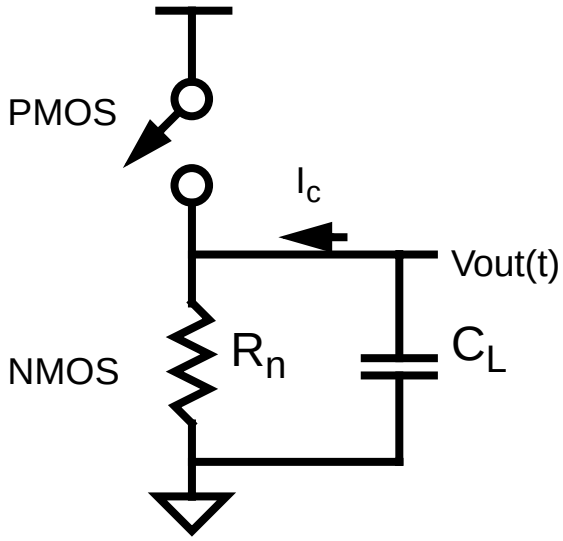
Inverter Switching

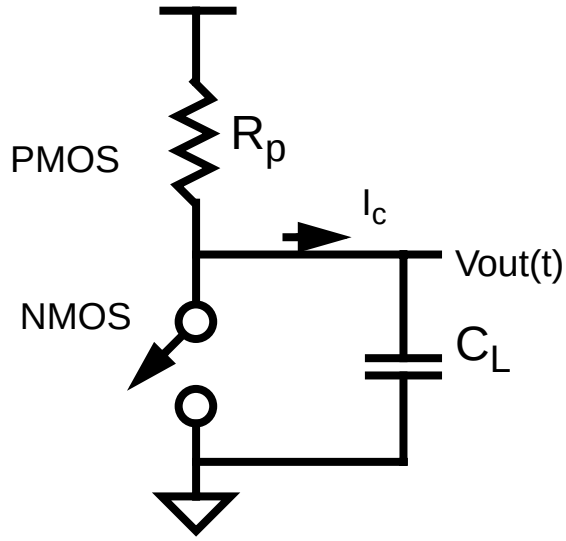


Inverter Rise/Fall Time

Simplifications:

$$t_f = k\frac{C_L}{\beta_n V_{DD}} = R_n C_L = \tau_f \qquad t_r = k\frac{C_L}{\beta_p V_{DD}} = R_p C_L = \tau_r$$





Inverter Sizing

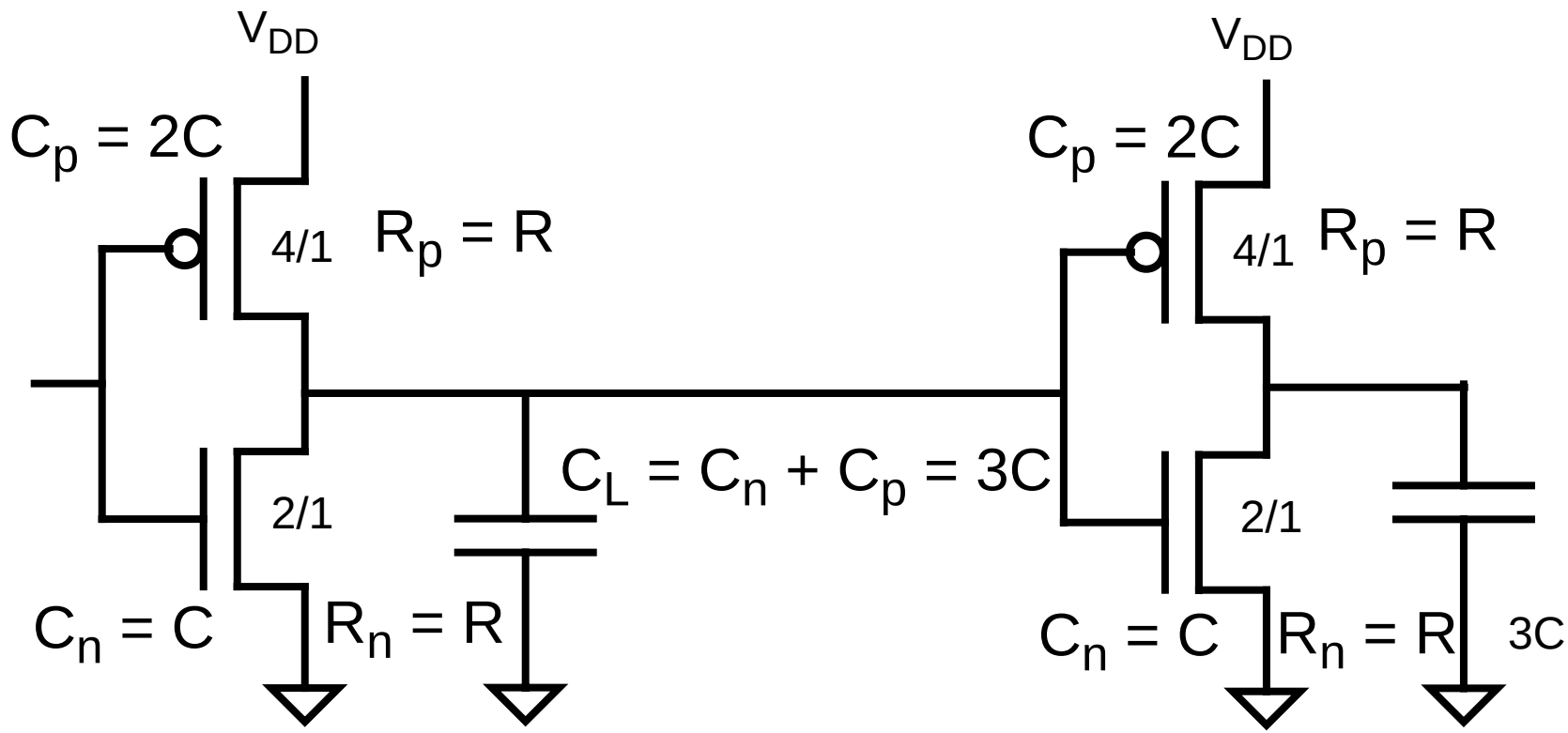
- Fall, Rise times:

$$\left(t_f = k\frac{C_L}{k_n\left(\frac{W}{L}\right)_n V_{DD}} \right), \left(t_r = k\frac{C_L}{k_p\left(\frac{W}{L}\right)_p V_{DD}} \right)$$

- To equalize rise, fall times:

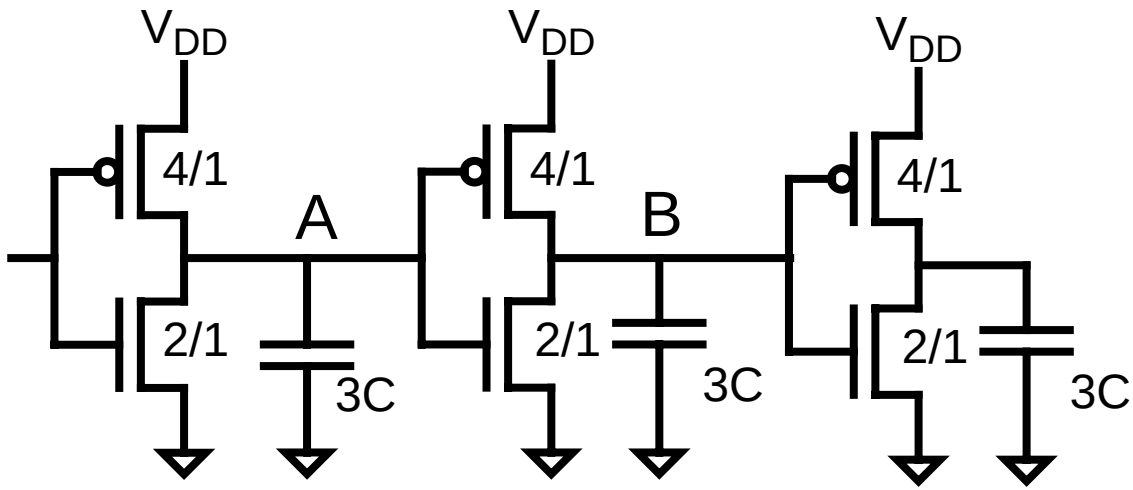
$$(\mu_n = 2\mu_p) \Rightarrow \left(\left(\frac{W}{L}\right)_p \approx 2\left(\frac{W}{L}\right)_n \right)$$

Inverter Sizing



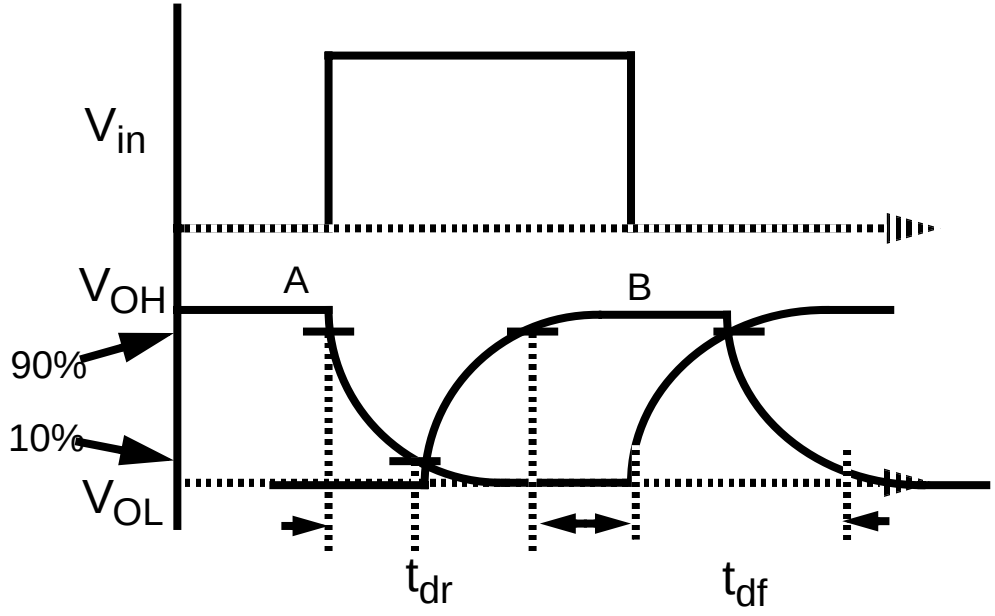
$$t_f = t_r = 3RC$$

Transistor sizing: Cascaded inverters



$t_{dr} = t_{f1} + t_{r2}$

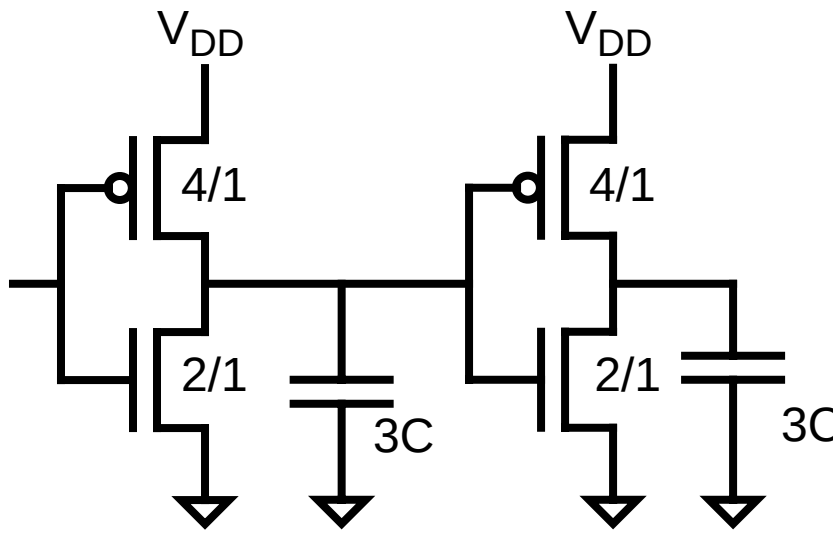
$t_{df} = t_{r1} + t_{f2}$



Transistor sizing: Cascaded inverters

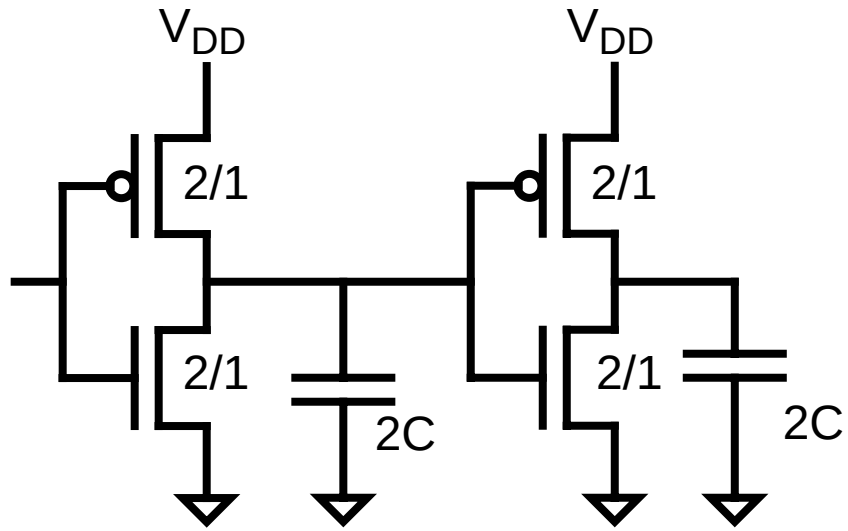
- t_{df} = R3C + R3C = 6RC

  t_{dr} = R3C + R3C = 6RC



- t_{df} = 2R2C + R2C = 6RC

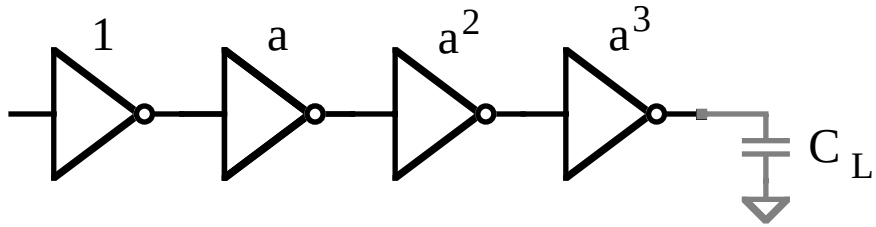
  t_{dr} = R2C + 2R2C = 6RC



Stage Ratios

Problem:

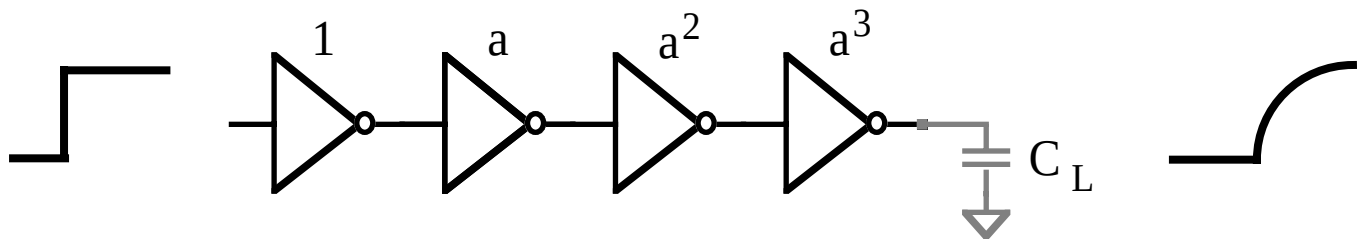
Driving large load capacitances (long buses, I/O pads)



Solution:

Inverter chain with stage ratio a= 2 - 5

Stage Ratios



$t_{dr} = R(2aC) +$

$(2R/a)(2a^2C) +$

$(R/a^2)(2a^3C) +$

$(2R/a^3)(C_L)$

$= 8RaC + 2RC_L/a^3$

$C_L = 100\ C$

for a = 1, $t_{dr} = 208RC$

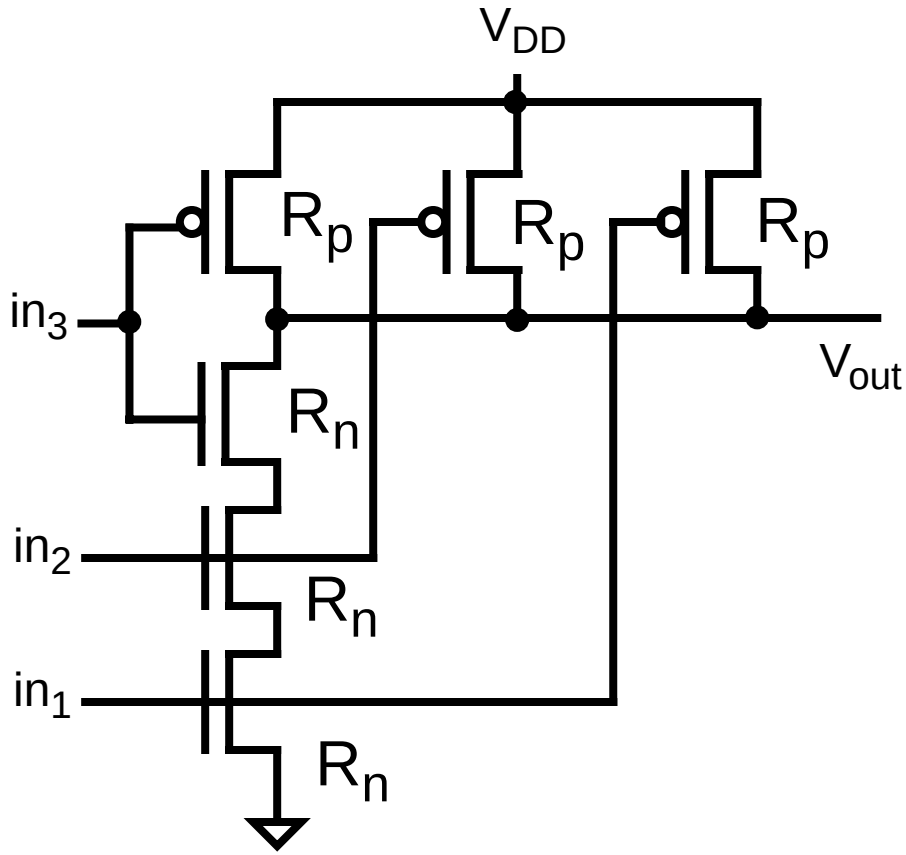
for a = 2, $t_{dr} = 41RC$

Sizing multi-input gates

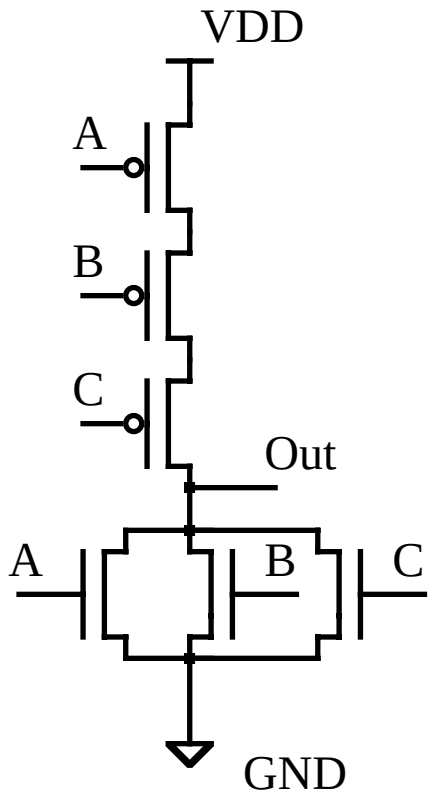
$$t_f = k\frac{C_L}{\frac{\beta_n}{3}V_{DD}}$$

$t_f = 3R_nC_L$

$t_r = R_pC_L$



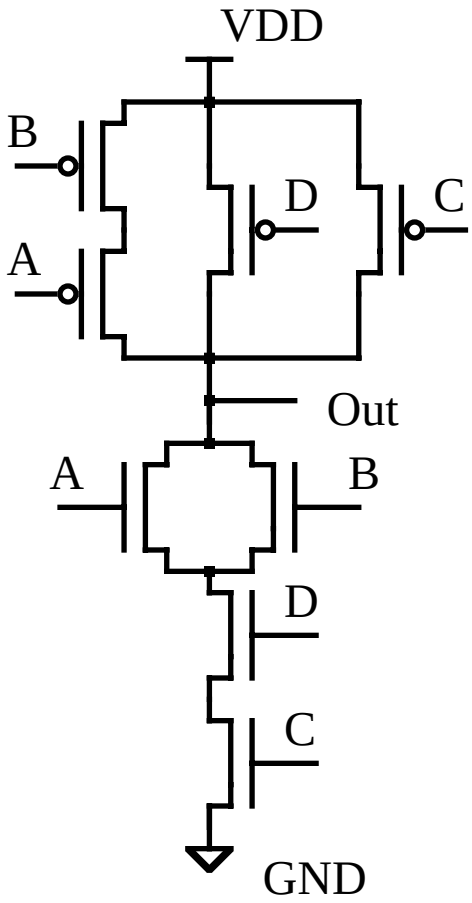
Sizing multi-input gates



$t_f = R_n C_L$

$t_r = 3R_p C_L$

Sizing complex gates



$t_f = 3R_nC_L$

$t_r = 2R_pC_L$