Carnegie Mellon
Electrical & Computer ENGINEERING

Version 3.

ECE 18-760 FALL 2001
VLSI CAD: Logic to Layout

FACULTY	Rob A. Rutenbar	HH 3105	x8-3334	rutenbar@ece.cmu.edu
COURSE SECRETARY	Lyz Knight	HH 3107	x8-5087	lyz@ece.cmu.edu
TEACHING ASSISTANT	Amit Singhee	HH 3104	x8-6646	asinghee@ece.cmu.edu

MEETING TIMES Tuesday, Thursday 12:30 - 2:20pm, HH B131

CLASS WEB PAGE **http://www.ece.cmu.edu/~ee760**

PRE-REQUISITES

Necessary Background	*Comments about Assumed Skills*
15-211, 15-212	Basic CS data structures and algorithms, programming in C language, UNIX
18-240	Basic digital design and verification, with combinational and sequential logic
Some exposure to VLSI ideas	18-321 or 18-322, or by permission

TEXTBOOKS **Synthesis and Optimization of Digital Circuits**, McGraw-Hill, 1994, G. De Micheli. Also, extensive lecture notes will be provided.

INTENDED AUDIENCE Graduate students and serious seniors interested in a broad exposure to the ideas behind the design of the algorithms inside VLSI CAD tools for logic and layout.

ASSIGNMENTS

Assignment	**Description**	**% of Grade**
6 Homeworks	Analysis & design of algorithms and small programs that illustrate core CAD ideas	40%
3 Projects	Programming assignments (JAVA/C++/UNIX) to build CAD tools	45%
3 Paper reviews	Analysis of topics from current CAD literature	15%

WHAT 18-760 IS NOT A circuits class. A design class where you mostly use other people's CAD tools. Another class involving only mindless hacking (as opposed to thinking). Math-free, i.e., there's some discrete math in this class, and some continuous math.

WHAT 18-760 IS An applied algorithms class. A class where you get to look inside CAD tools and see what makes them work. A natural bridge between CE and CS applications and ideas. A class where you get to build (simplified chunks of) VLSI CAD tools. A good course for would-be CAD folks, or would-be VLSI designers, or folks just interested in nice algorithms that deal with 1s and 0s, graphs, time & waveforms, polygons.

TENTATIVE SYLLABUS (i.e., things *may* change...)

			HW	Proj	Paper
WEEK 1	**8/28**	Introduction to CAD flow of ICs; Advanced Boolean Algebra			
	8/30	Advanced Boolean Algebra, cont.			
WEEK 2	**9/4**	Advanced Boolean Algebra, cont.			
	9/6	JAVA Language Review	**hw1**		
WEEK 3	**9/11**	Boolean Representation: BDDs			
	9/13	Boolean Representation: BDDs, cont			
WEEK 4	**9/18**	Boolean Representation: BDDs, cont			
	9/20	Formal Verification: Finite State Machine Equiv	**hw2**		
WEEK 5	**9/25**	Formal Verification: FSM Equivalence, continued		**Proj1**	
	9/27	2-Level Logic Synthesis: ESPRESSO			
WEEK 6	**10/2**	2-Level Logic Synthesis: ESPRESSO, cont.			**Pap1**
	10/4	Multilevel Logic Synthesis: Boolean Network Model	**hw3**		
WEEK 7	**10/9**	Multilevel Logic Synthesis: Algebraic Division			
	10/11	Project 2 Review			
WEEK 8	**10/16**	Multilevel Logic Synthesis: Rectangle Covering			
	10/18	Multilevel Logic Synthesis: Rectangle Covering, cont			
WEEK 9	**10/23**	Multilevel Logic Synthesis: Role of Don't Cares		**Proj2**	
	10/25	Technology Mapping	**hw4**		
WEEK 10	**10/30**	Component Placement for ASICs			
	11/1	Component Placement for ASICs, cont			**Pap2**
WEEK 11	**11/6**	Component Placement for ASICs, cont **RAR away; guest lec**			
	11/8	Component Routing for ASICs			
WEEK 12	**11/13**	Project 3 Review			
	11/14	Component Routing for ASICs, cont			
WEEK 13	**11/20**	Static Timing Analysis.	**hw5**		
	11/22	NO CLASS--THANKSGIVING BREAK		**Proj3**	
WEEK 14	**11/27**	Static Timing Analysis, cont. **RAR away; guest lecs**			**Pap3**
	11/29	Electrical Delay Analysis			
WEEK 15	**12/4**	Geometric Data Structures for Analysis & Verification	**hw6**		
	12/6	Geometric Data Structures, cont. **RAR away; guest lec**			
WEEK 16	**12/11**	Geometric Data Structures, cont.			

note revised deadlines here