(Lec 14) Placement & Partitioning: Part III

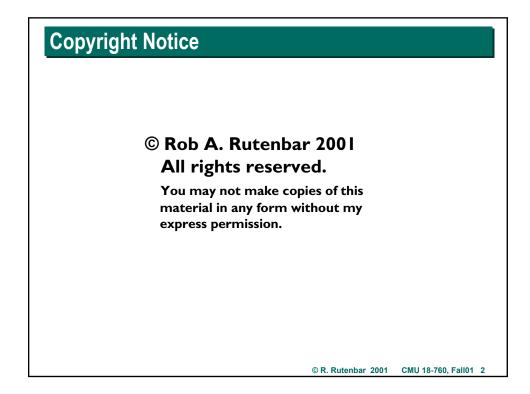
What you know

- ▶ That there are 3 big placement styles: iterative, recursive, direct
- > Placement via iterative improvement using simulated annealing
- ► Recursive-style placement via min-cut with F&M partitioning

What you don't know

- ► The last style: direct placement
- ► One issue is mathematical model: quadratic wirelength minimization
- Second issue is legalization strategy: we do **PROUD**-style legalization

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Where Are We?



	Μ	Т	W	Th	F	
Aug	27	28	29	30	31	1
Sep	3	4	5	6	7	2
	10		12	13	14	3
	17	18	19	20	21	4
	24	25	26	27	28	5
Oct		2	3	4	5	6
	8	9	10		12	7
	15	16	17	18	19	8
	22	23	24	25	26	9
	29	30	31	1	2	10
Nov	5	6	7	8	9	11
	12	13	14	15	16	12
Thnxgive	19	20	21	22	23	13
	26	27	28	29	30	14
Dec	3	4	5	6	7	15
	10		12	13	14	16

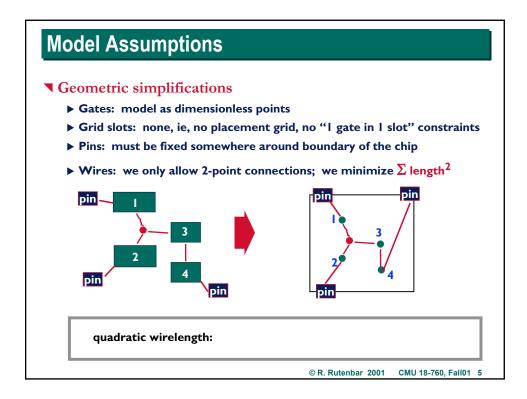
Introduction Advanced Boolean algebra JAVA Review Formal verification 2-Level logic synthesis Multi-level logic synthesis Technology mapping

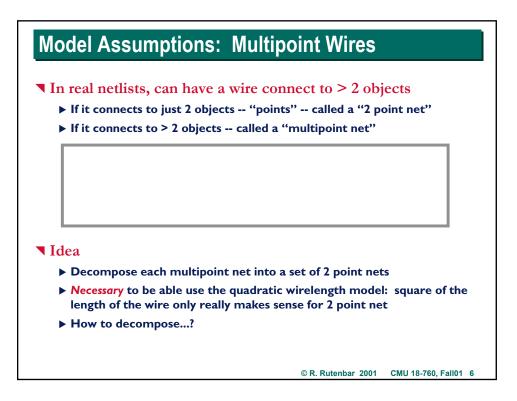
Placement

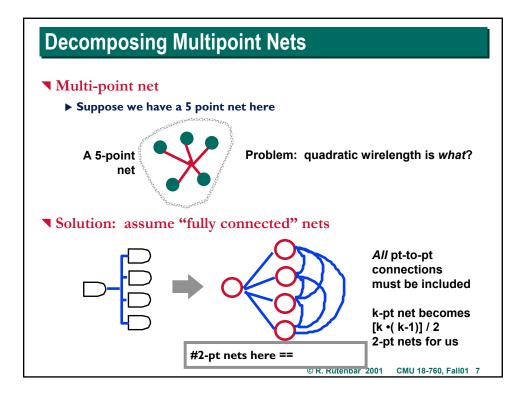
Routing Static timing analysis Electrical timing analysis Geometric data structs & apps

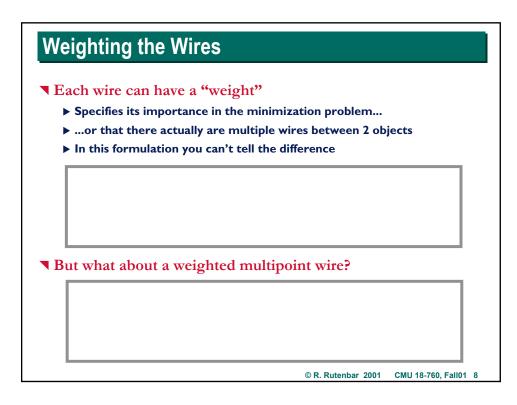
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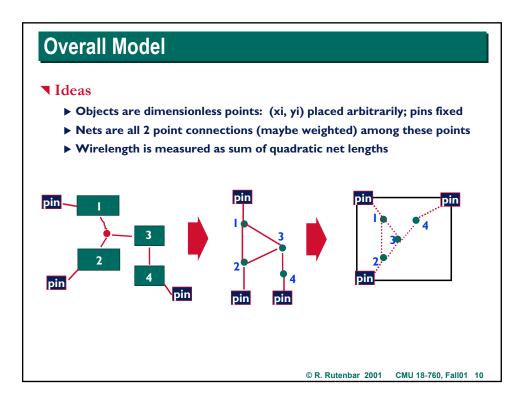


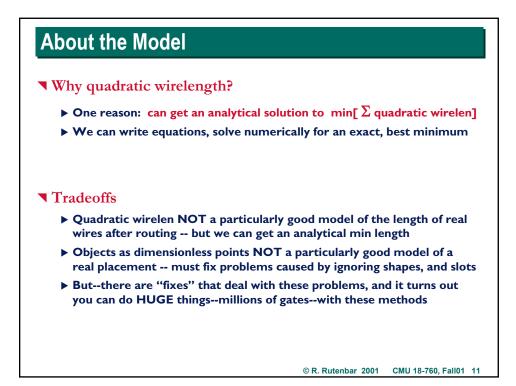
Weighting the Wires

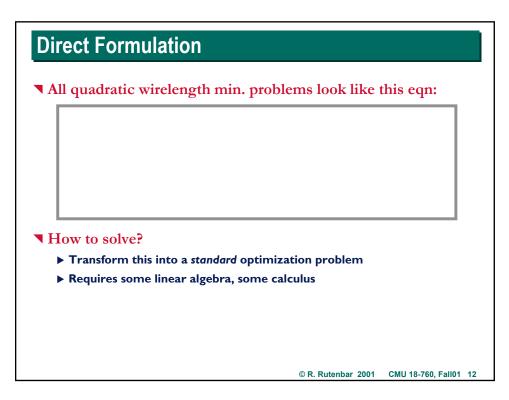
Question

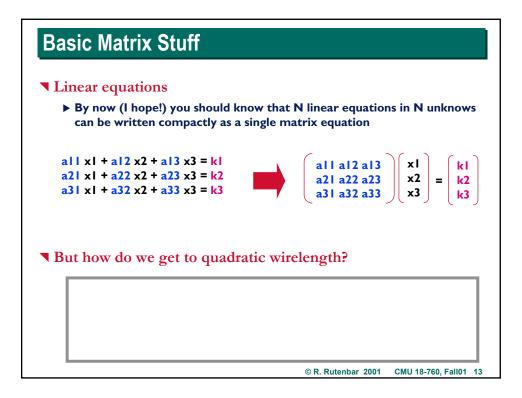
- When we decompose, what happens to the weights?
- Solution: for k-point net, multiply each 2 pt connection by
- **Example: 4 point net, look at typical partition of it objects**

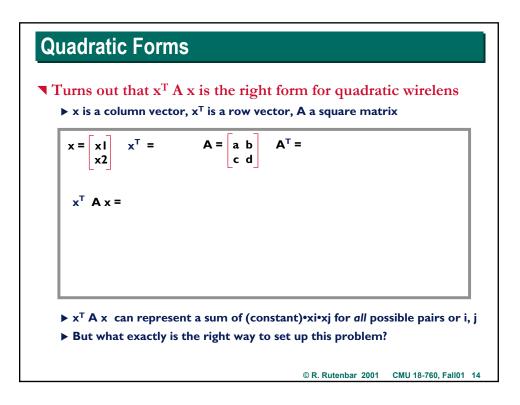


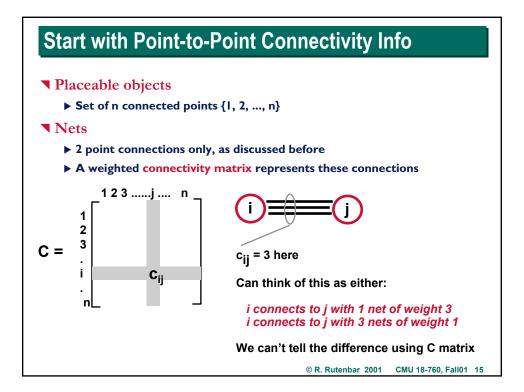


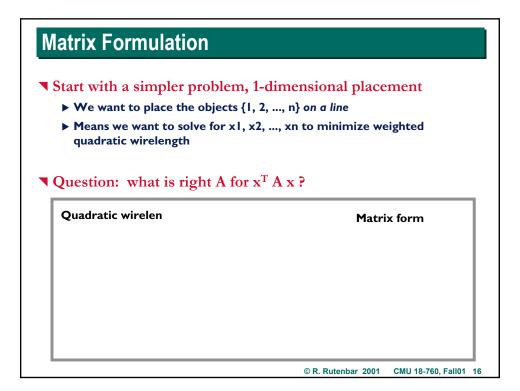


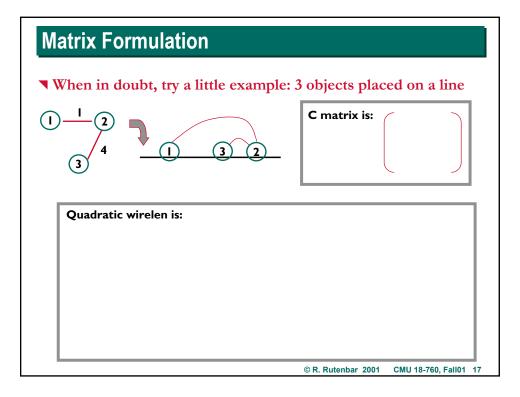


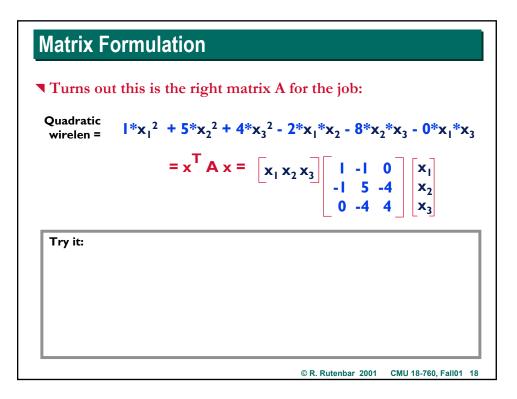


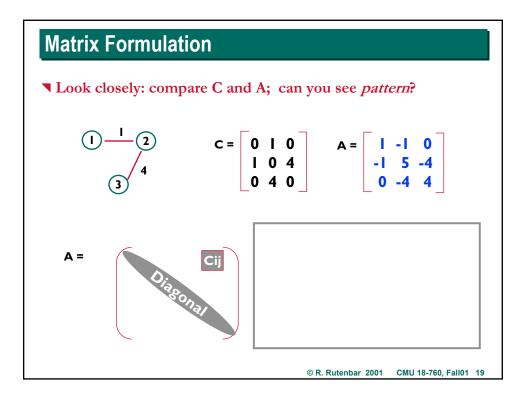


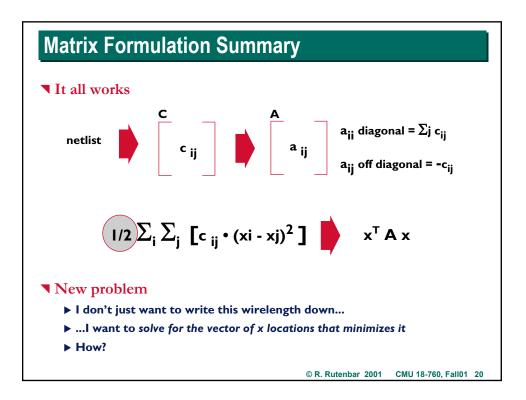




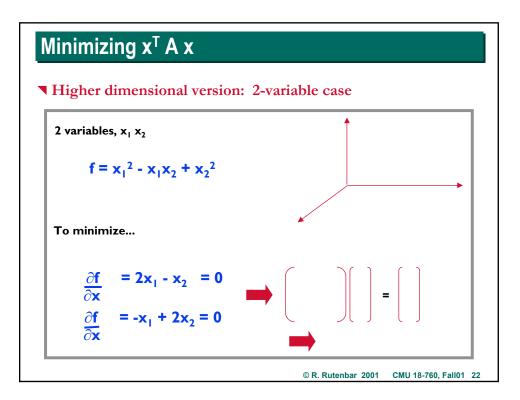


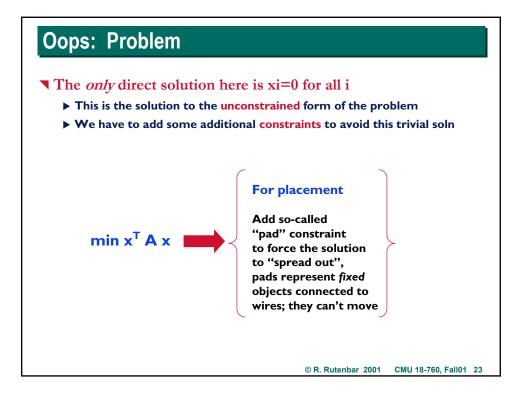


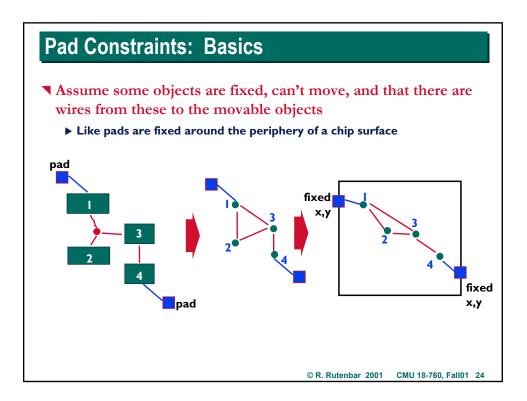


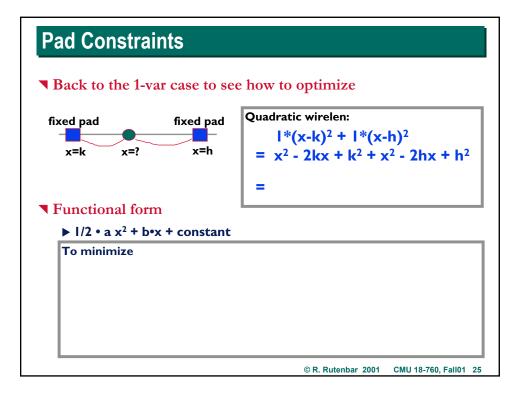


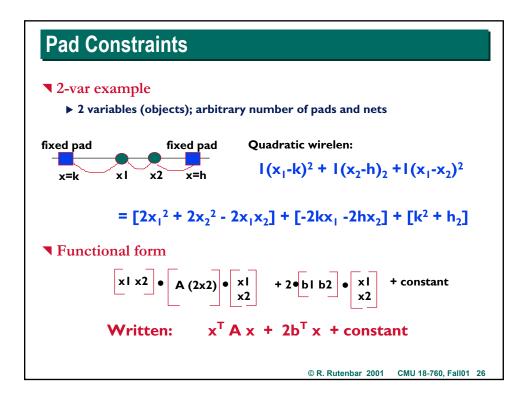
Minimizing x ^T A x						
S	 This minimization is just a higher dimensional version of something you already should know 1-variable version 					
	Just one variable, x		1			
	To minimize	•				
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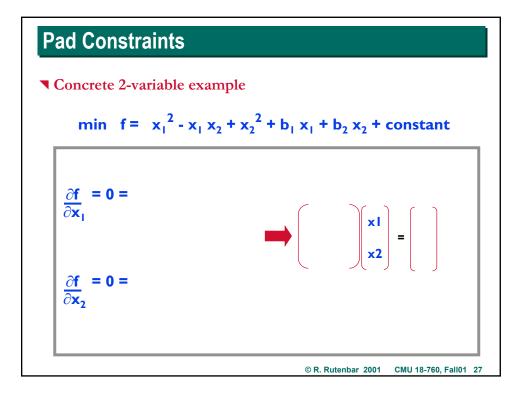


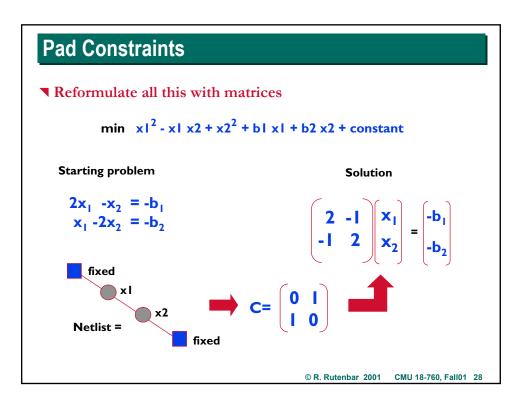


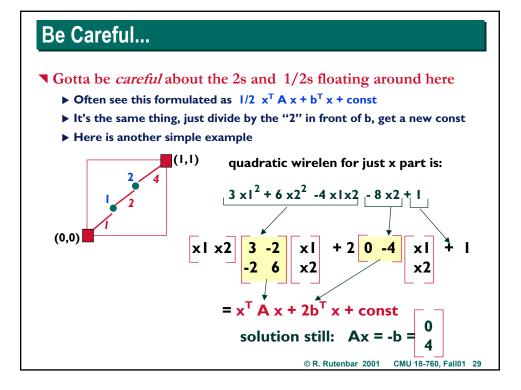


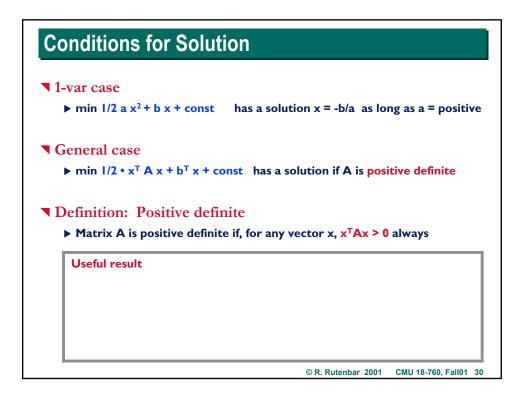


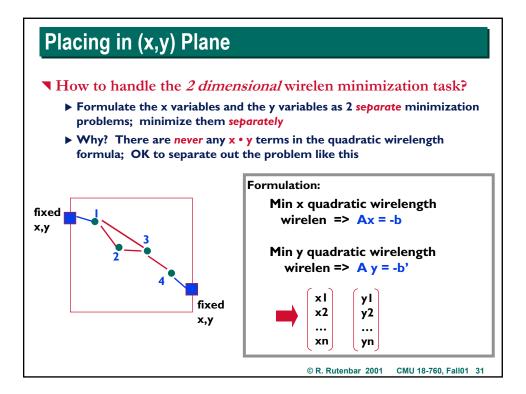


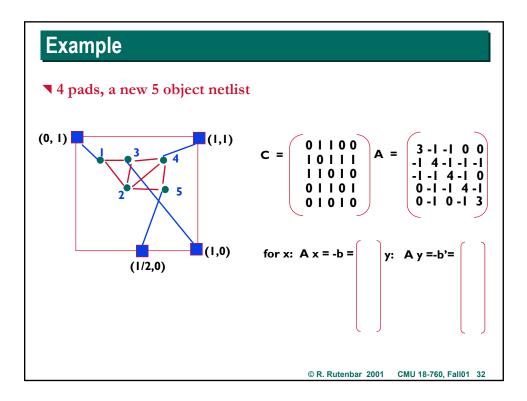


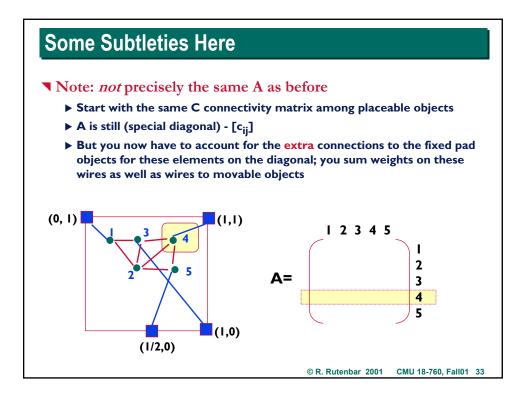


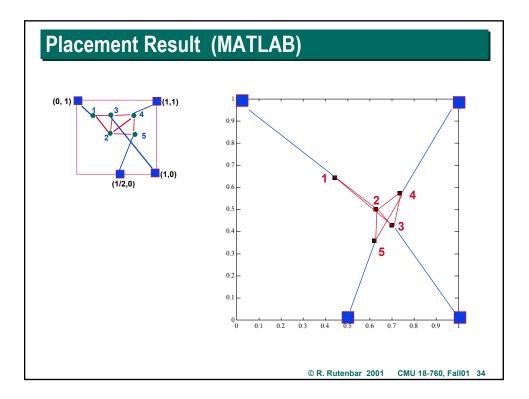


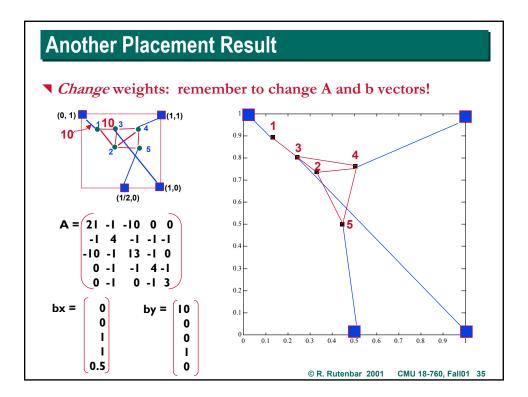












Summary So Far...

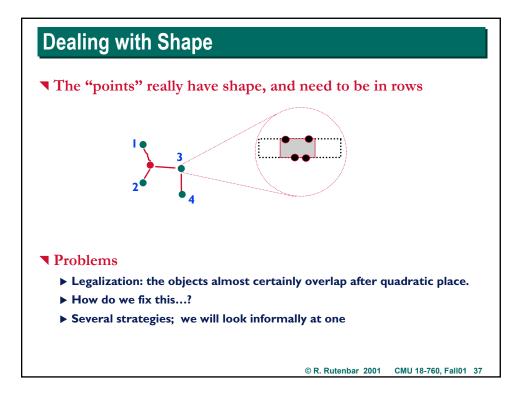
Direct placement

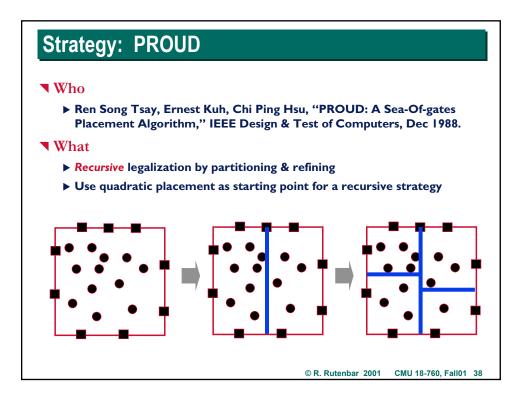
- Dimensionless points, 2-point weighted wires
- Minimize sum of squares of wire lengths
- ► Has a direct-form representation of aggregate wirelength with functional form
 - $I/2 \cdot x^T A x + b^T x + const$ or equivalently
 - $x^{T} A x + 2 b^{T} x + const$
- ...this is minimized at Ax = -b
- ► Do x and y placements separately

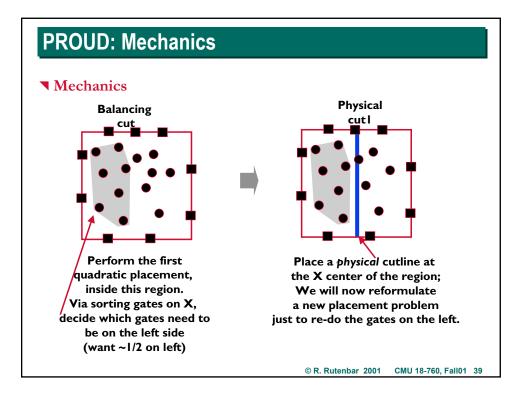
Open issues

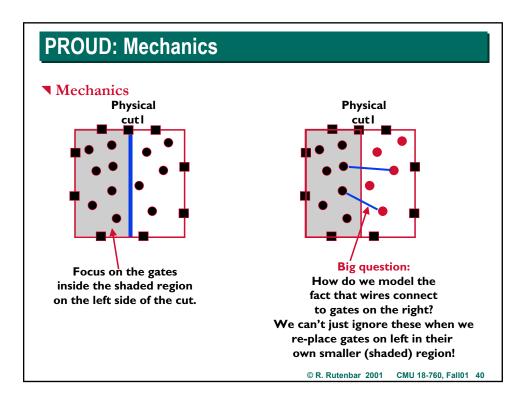
- ► These objects are really not dimensionless points, and we don't yet have a legal placement when this is finished
- ► There are ways around these problems

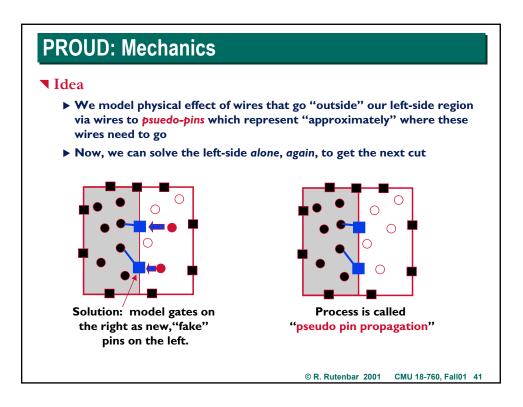
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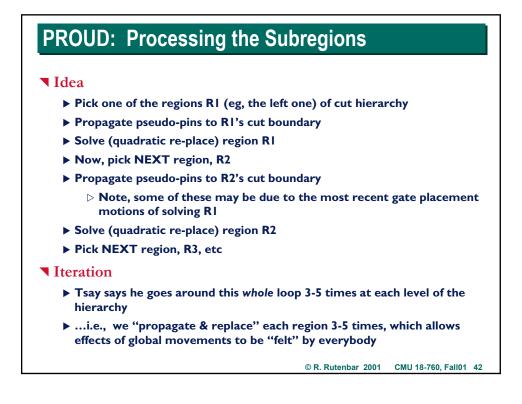


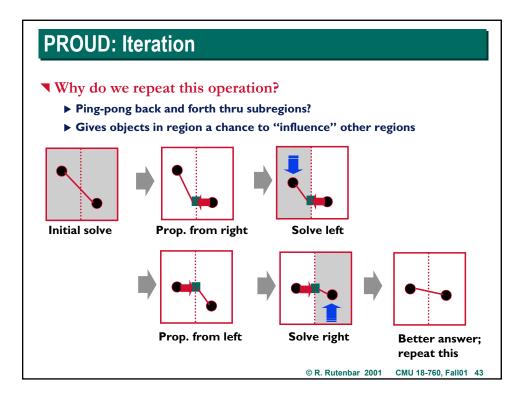


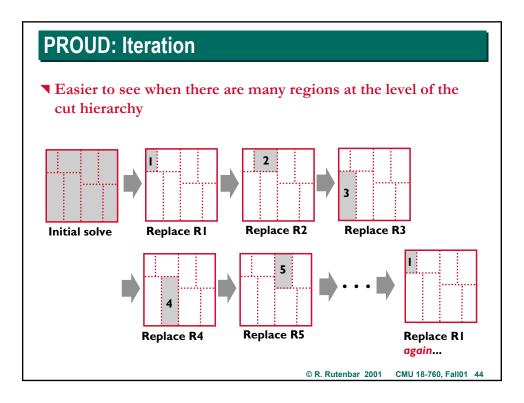


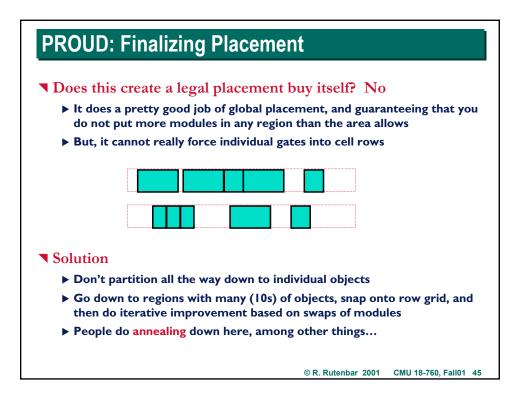


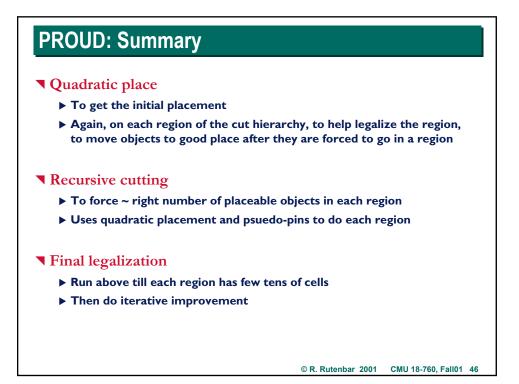












Summary

■ Iterative improvement placement by annealing

• "The" approach in the 1980s; runs out of gas at a few 100,000 gates

Recursive mincut placers

- ▶ Based on clever, iterative improvement partitioning
- Coming back into style today; very good for very large ASICs

Quadratic direct placement

- > Point-based, 2-point-wires; can minimize quadratic wirelen exactly, fast
- But, placement not really legal (overlaps); lots of work here.

■ Today

- Mix of quadratic and mincut techniques to do "gross" placement; iterative improvement "local refinement" to get legal final placement
- ► This is really how people really do millions of gates today... © R. Rutenbar 2001 CMU 18-760, Fall01 47