

MOSFET transistor I-V characteristics

Linear region: $i_D = K[2(v_{GS} - V_t)v_{DS}]$
 $v_{DS} \ll v_{GS} - V_t$

$$K_n = C_{ox}\mu_n$$

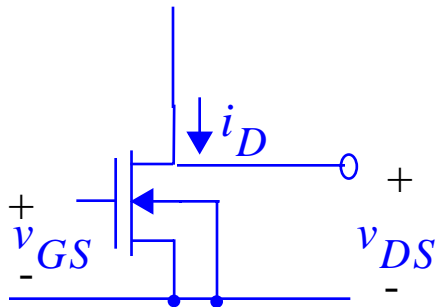
$$K = \frac{W}{2L}K_n$$

Triode region: $i_D = K[2(v_{GS} - V_t)v_{DS} - v_{DS}^2]$
 $v_{DS} < v_{GS} - V_t$

$$v_{DS}|_{sat} = v_{GS} - V_t$$

(current) Saturation region: $i_D = K[(v_{GS} - V_t)^2](1 + \lambda v_{DS})$

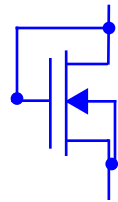
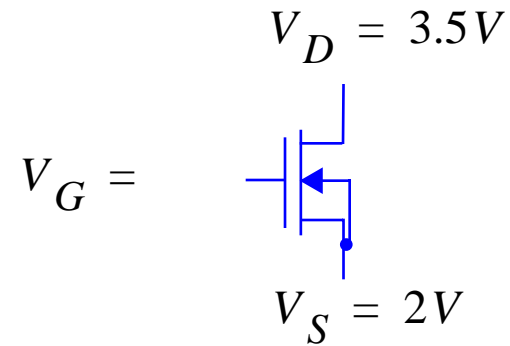
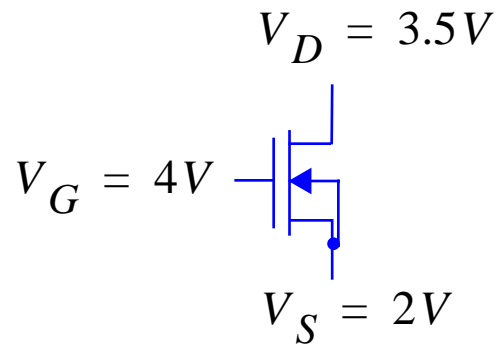
$$v_{DS} \geq v_{GS} - V_t$$



Is the transistor in saturation region?

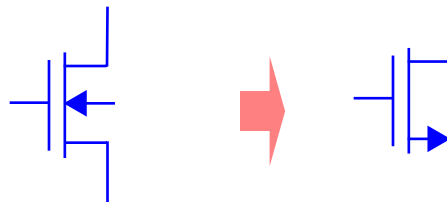
$$v_{DS}|_{sat} = v_{GS} - V_t$$

$$V_t = 1V$$

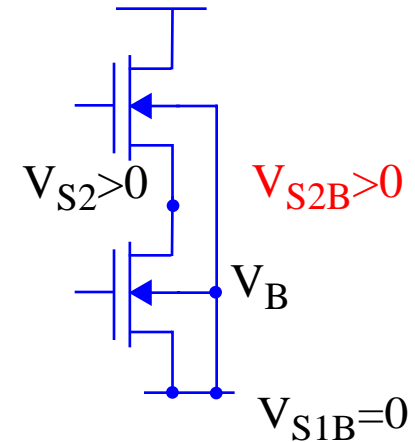
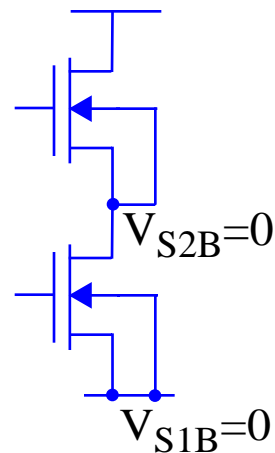


Body Effect

- The source and bulk will not be at zero volts all of the time
- The p-type bulk will be connected to the lowest supply voltage for an IC
- Discrete MOSFETs may have bulk tied directly to the source

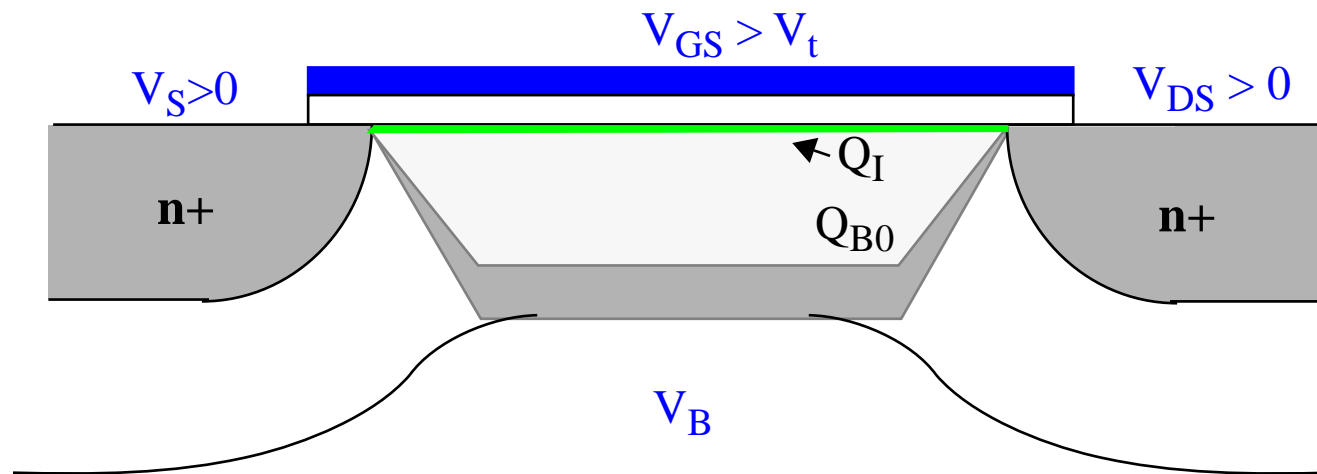


- But for ICs we can assume that there can be a positive V_{SB} for NMOSFETs



Body Effect

- Positive V_{SB} for NMOSFETs tends to increase Q_B , hence decrease Q_I , for a fixed V_{GS}



Body Effect

- Modeled as a change in the threshold voltage as a function of V_{SB}
- The source is, by definition for NMOSFET, at a lower positive potential than the drain, which is why we use it as our reference voltage

$$V_t = V_{t0} + \gamma(\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f})$$

- SPICE will calculate this variation in threshold voltage, or you can over-ride its calculation by directly specifying **gamma**

Temperature Variations

- The threshold voltage varies with temperature due to carrier generation in the substrate --- tends to decrease with increasing temperature
 - ~2mV for every 1°C increase

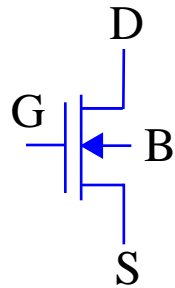
$$V_t = V_{t0} + \gamma(\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f})$$

- K also changes with temperature due to change in mobility
 - Tends to dominate temperature variation for large i_D
- $$I \propto \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (v_{GS} - V_t)^2$$
- Will i_D increase or decrease with temperature?

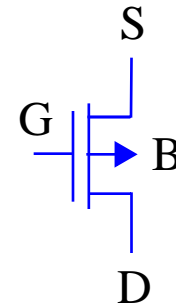
T₁

T₂ > T₁

Where is drain, where is source?



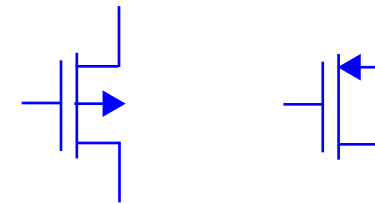
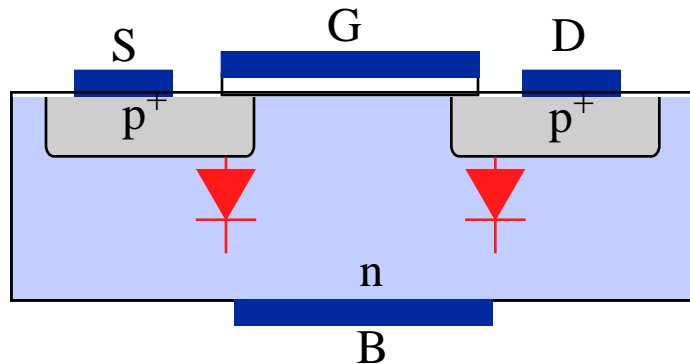
n-channel transistor



p-channel transistor

PMOSFETs

- All of the voltages are negative
- Carrier mobility is about half of what it is for n channels



- The bulk is now connected to the most positive potential in the circuit
- Strong inversion occurs when the channel becomes as p-type as it was n-type
- The inversion layer is a positive charge that is sourced by the larger potential and drained at the smallest potential
- The threshold voltage is negative for an enhancement PMOSFET
 - Note that the flatband voltage (which is negative) effects now tend to increase the PFET threshold while they decreased the NFET threshold

PMOS

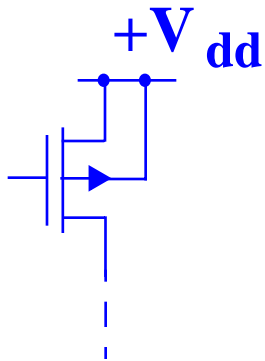
- The equations are the same, but all of the voltages are negative
- Triode region:

$$|v_{GS}| \geq |V_t| \quad |v_{DS}| \leq |v_{GS} - V_t|$$

$$i_D = K[2(|v_{GS} - V_t|)|v_{DS}| - v_{DS}^2] \quad |K| = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} \quad \left[\frac{A}{V^2} \right]$$

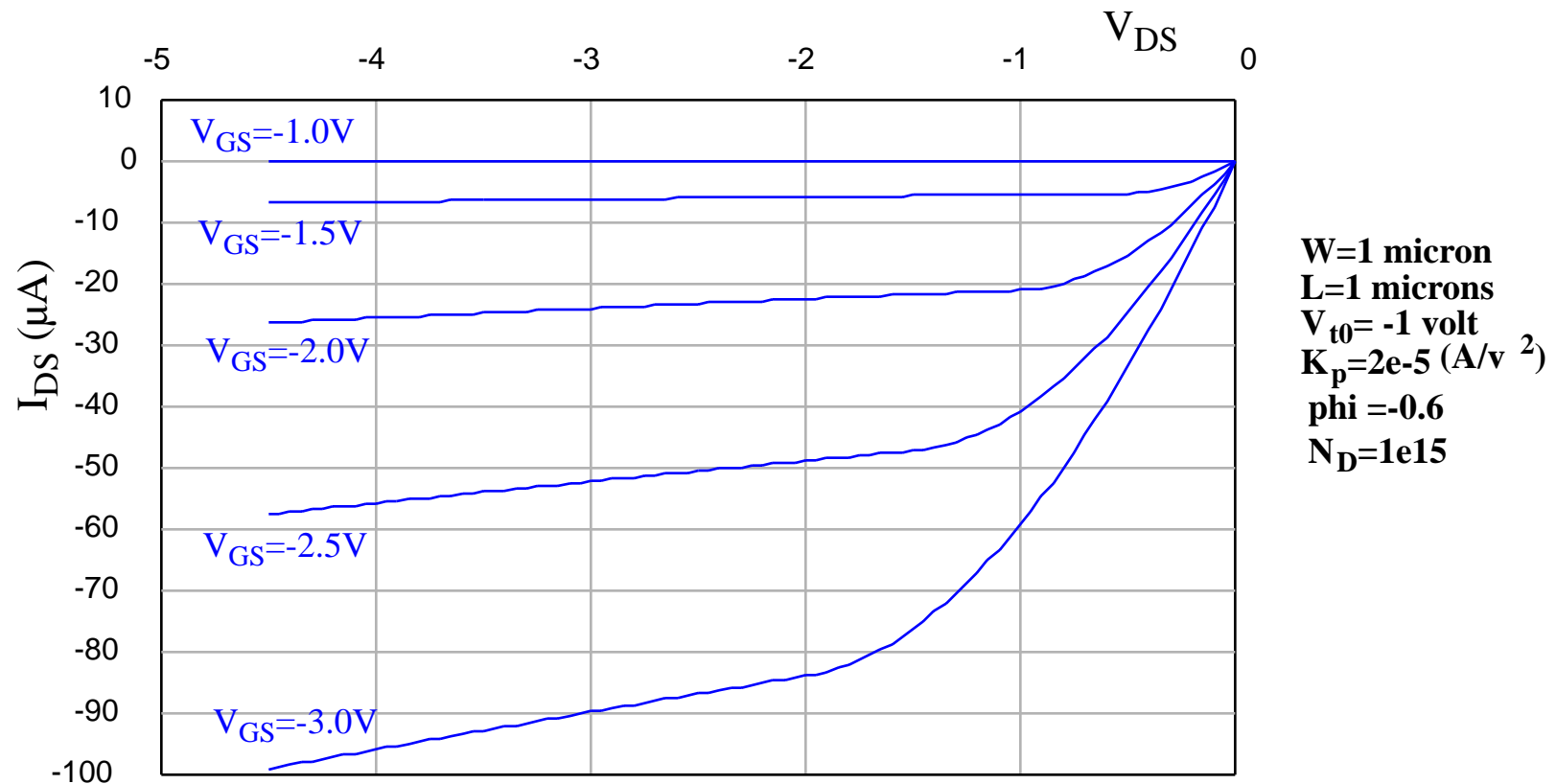
- i_D is also negative --- positive charge flows into the drain
- Saturation expression is the same as it is for NFETs:

$$i_D|_{sat} = K[(v_{GS} - V_t)^2](1 + \lambda|v_{DS}|)$$



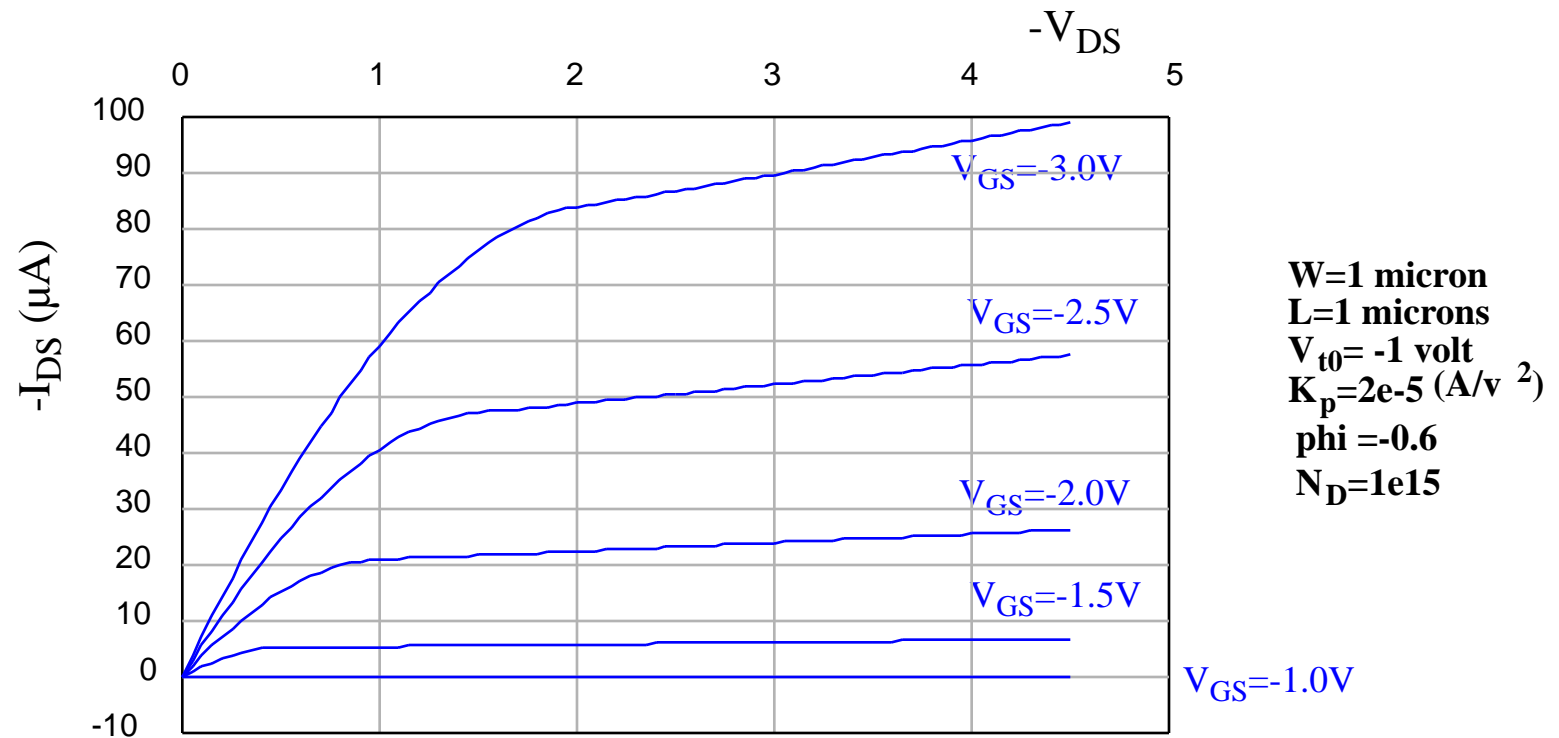
PMOS

- Characteristic appears to be the same, except that all of the voltages are negative



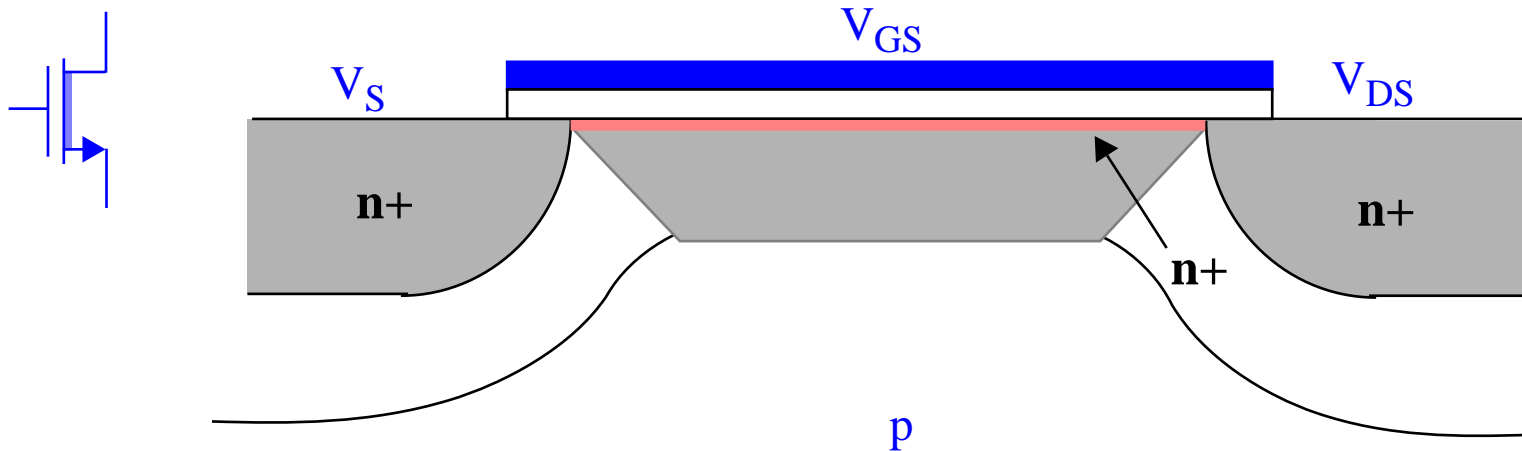
PMOS

- But it is generally displayed as:



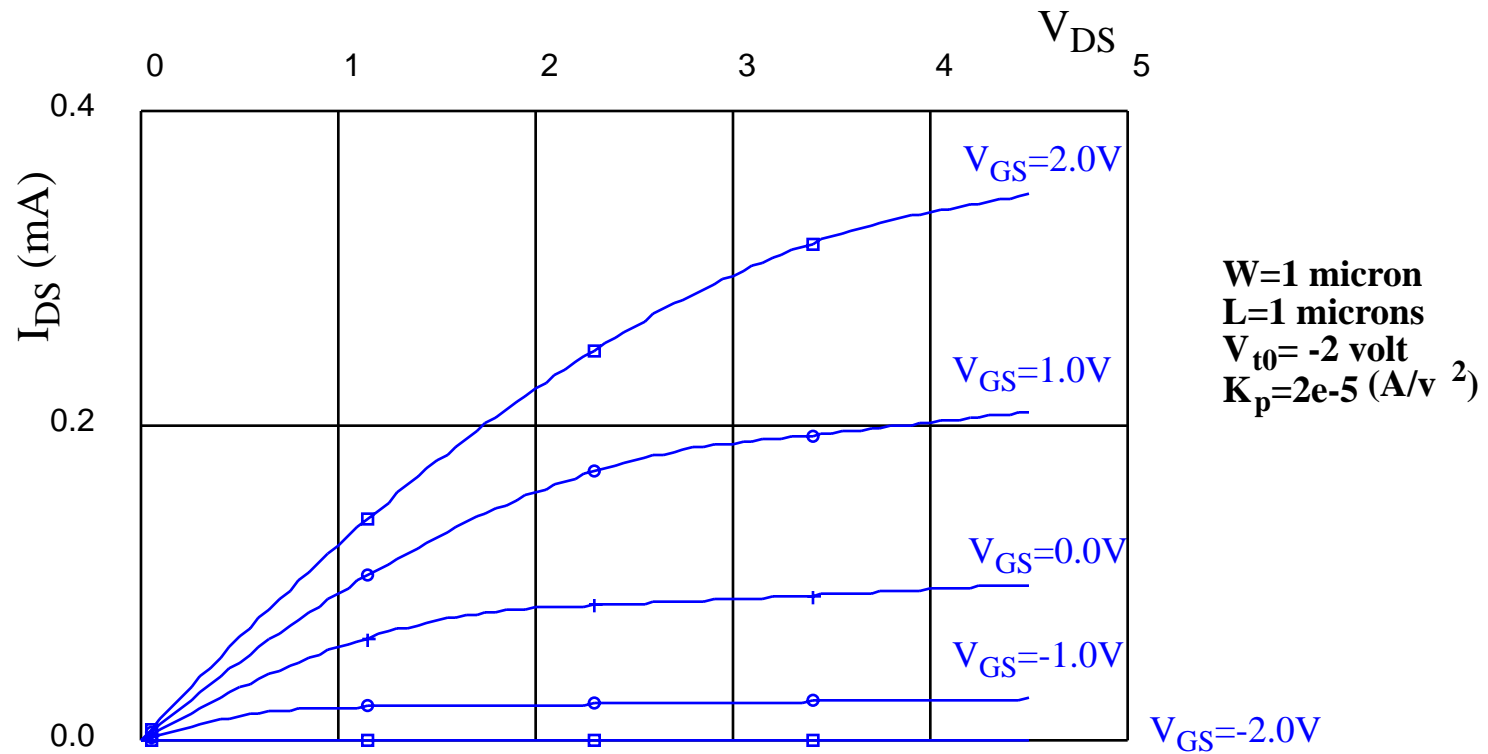
Depletion Mode NMOSFET

- Depletion mode FETs have a channel implanted such that there is conduction with $V_{GS}=0$
- The operation is the same as the enhancement mode FET, but the threshold voltage is shifted
 - V_t is negative for depletion NMOS, and positive for depletion PMOS



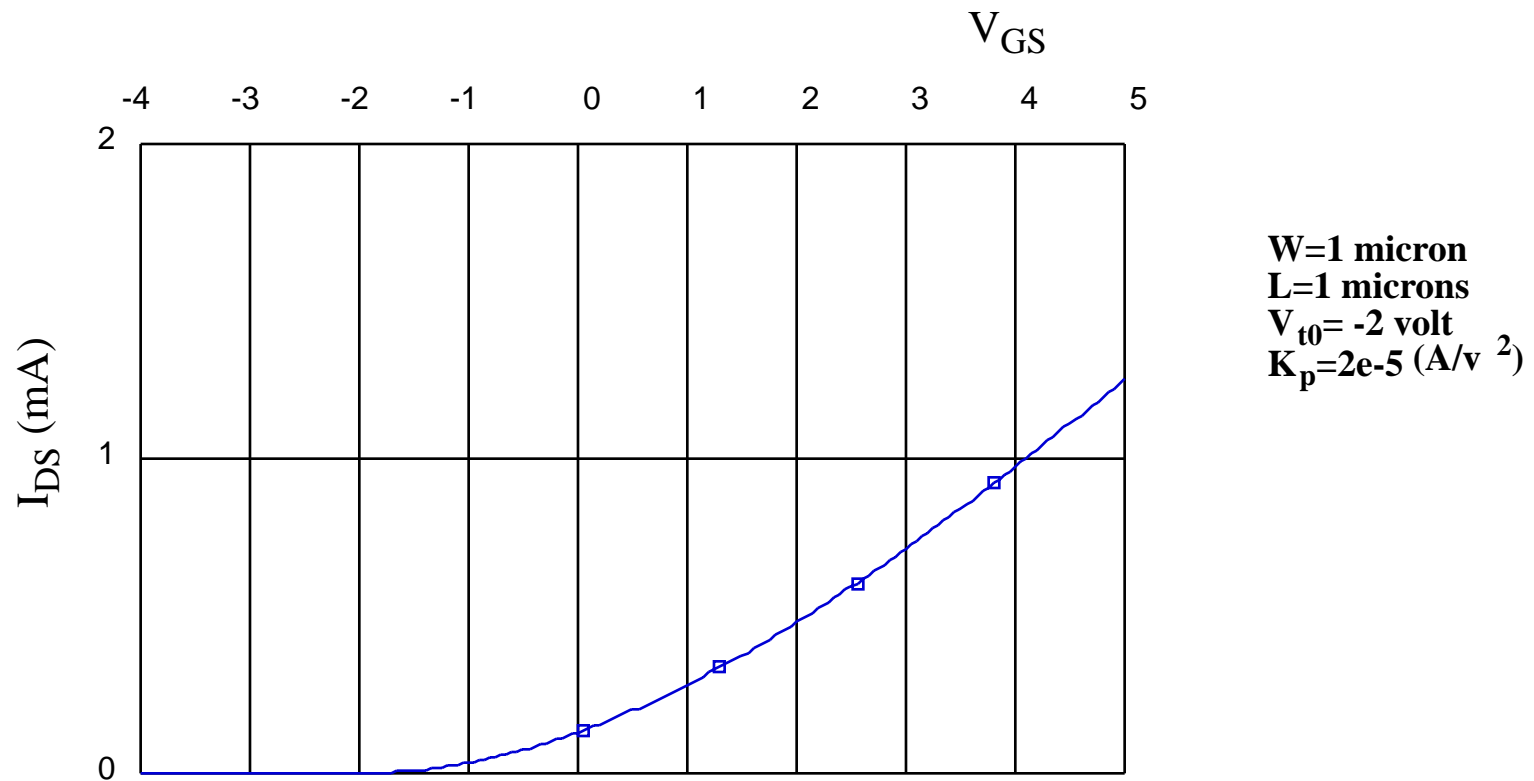
Depletion Mode NMOSFET

- Negative gate voltage is required to turn the channel off



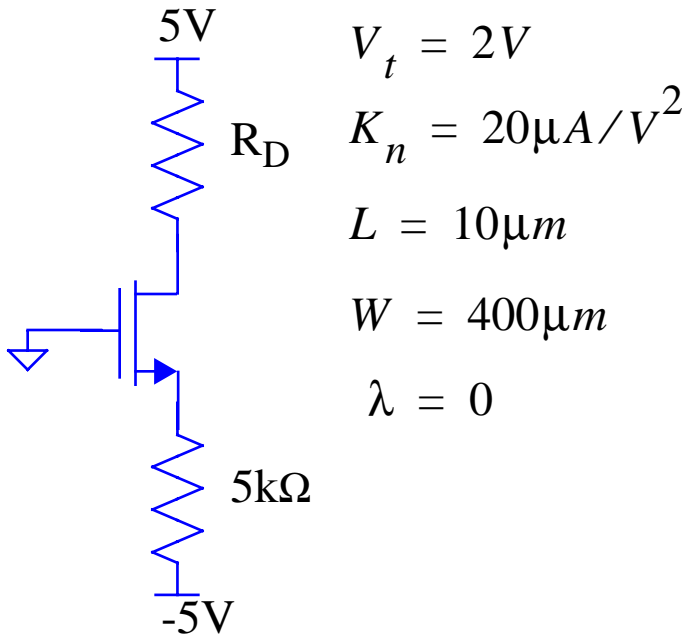
Depletion Mode NMOSFET

- The i_{DS} vs. v_{GS} characteristic is still quadratic in saturation



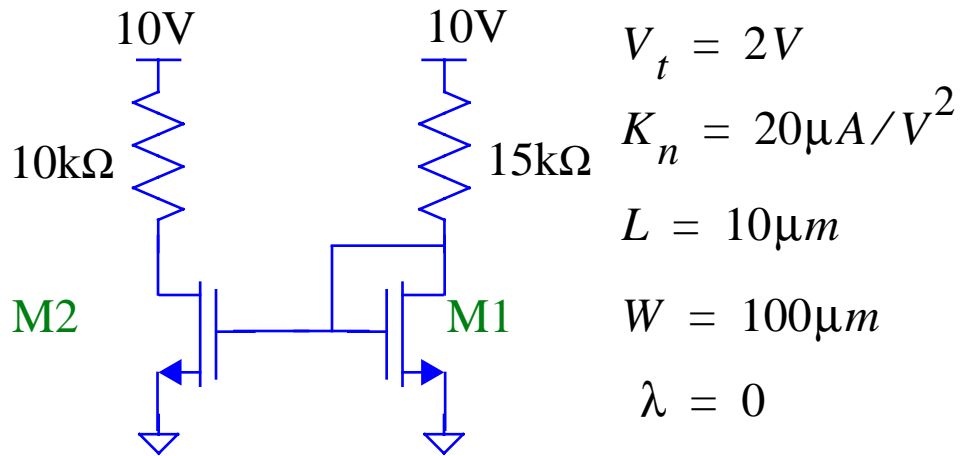
Examples

- Find the largest value that R_D can have before the transistor fails to operate in saturation



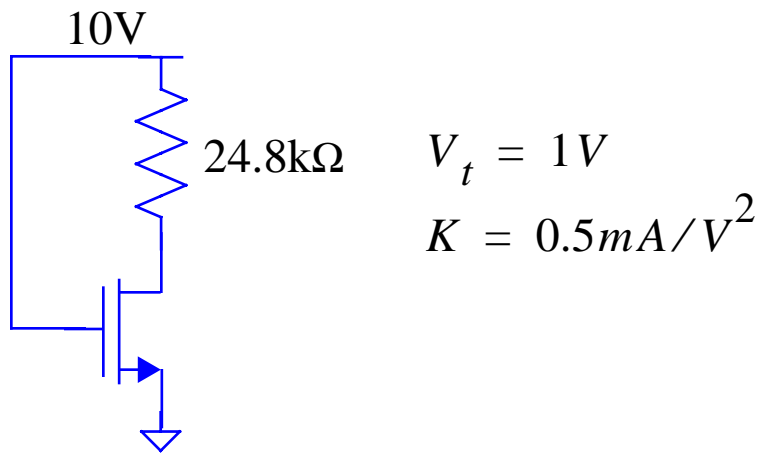
Examples

- Find the drain currents and voltages for both transistors



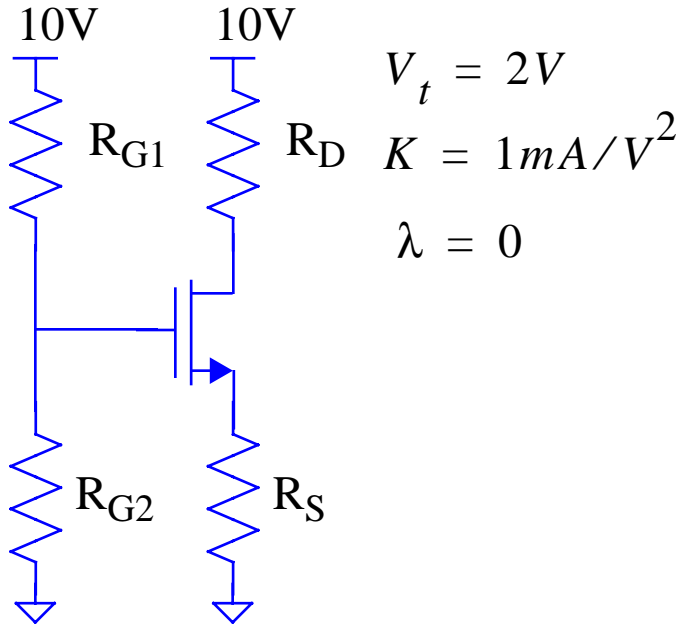
Examples

- What is the effective resistance of the transistor in the triode region?



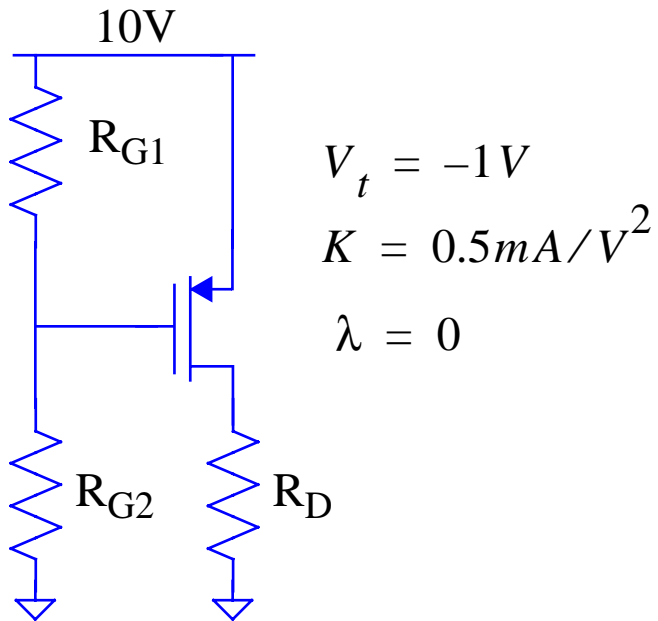
Examples

- Select the R's so that the gate voltage is 4V, the drain voltage is 4V and the current is 1mA.



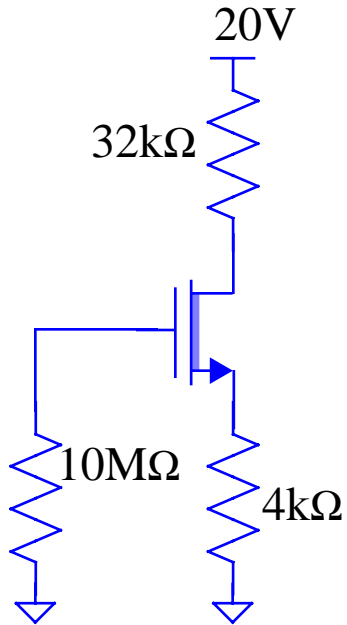
Examples

- Select the R's so that the transistor is in saturation with a drain current of 1.0mA and a drain voltage of 5V



Examples

- Solve for the drain current and voltage



$$V_t = -2V$$

$$K = 1mA/V^2$$

$$\lambda = 0$$