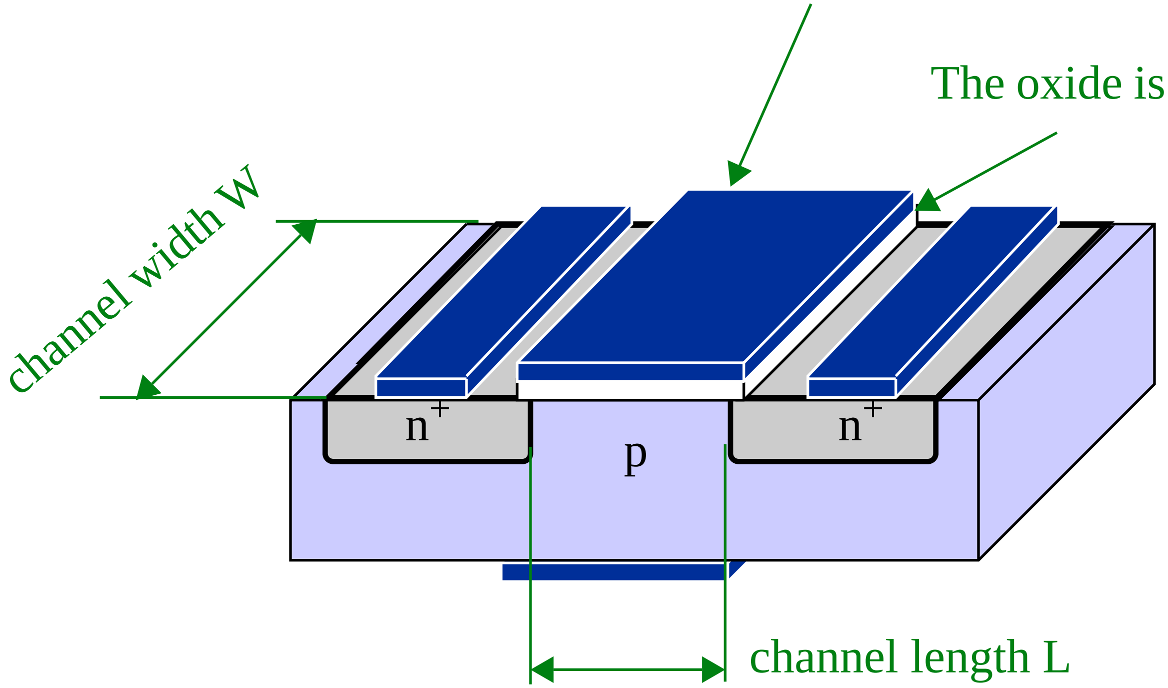
FETs: Field Effect Transistors

- MOSFETs: Metal-Oxide Semiconductor Field Effect Transistors
  - gates are really polysilicon, not metal
  - extremely large input resistance
  - four terminal devices
  - occupy less area than BJTs --- predominant technology for digital
  - but do not provide the same gain as BJTs for analog
- Used for analog mainly due to the need mixed-signal designs

- JFETs: Junction Field Effect Transistors
  - not as popular as MOSFETs, but behave very similarly

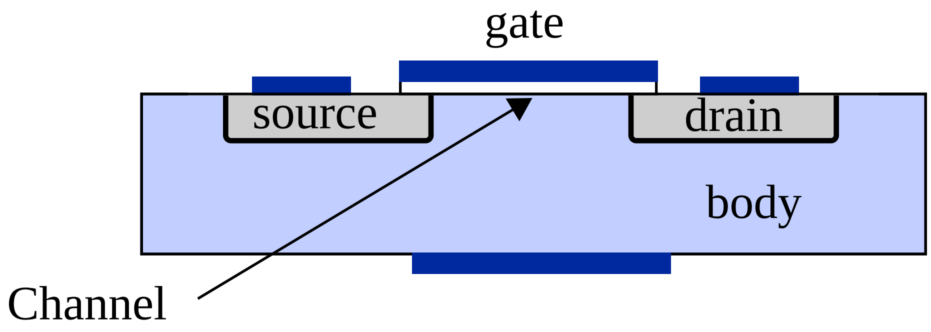
Enhancement Mode MOSFETs

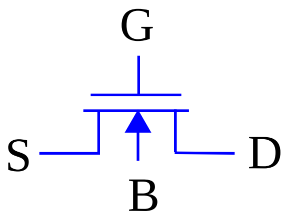
- The basic structure of an enhancement mode mosfet


Made of polysilicon or rarely metal.

The oxide is very thin: e.g. 40 - 15 nm.

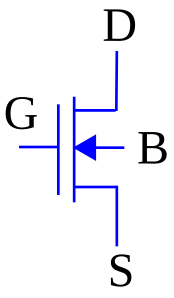
- Cross-section view



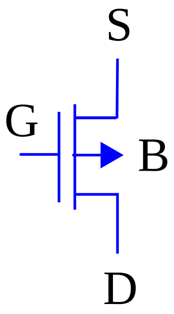


Enhancement Mode MOSFETs

- NOTE: 4 terminals!!!



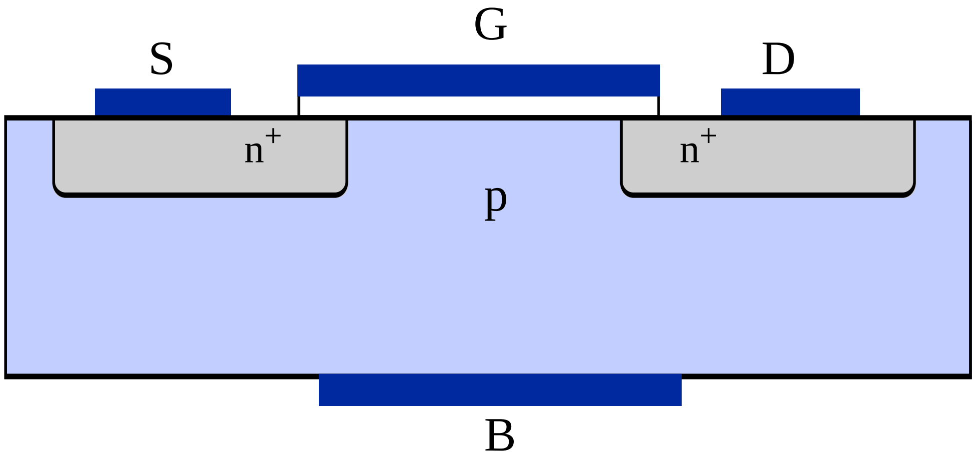
n-channel transistor
or N-MOSFET
(p-type substrate)



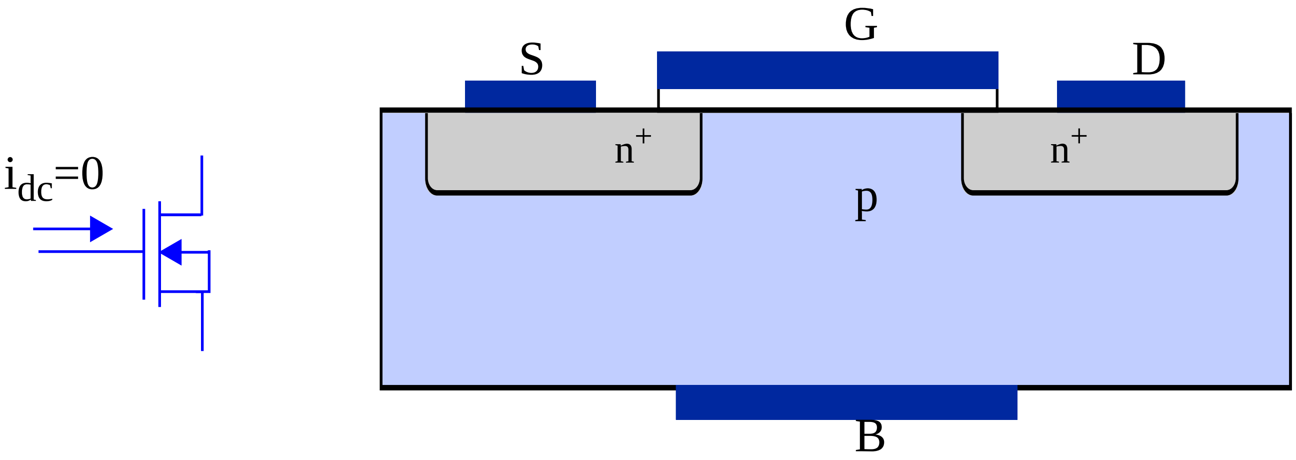
p-channel transistor
or P-MOSFET
(n-type substrate)

Enhancement Mode MOSFETs

- We keep the source and drain p-n junctions off at all times
- They contribute small leakage currents, and some nonlinear capacitance

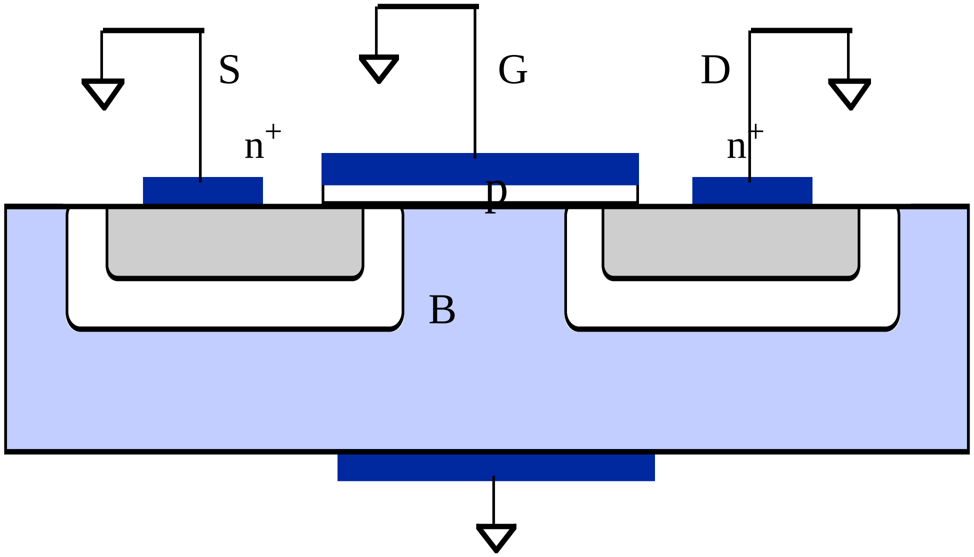


- The gate input has practically infinite resistance, and behaves like a capacitor

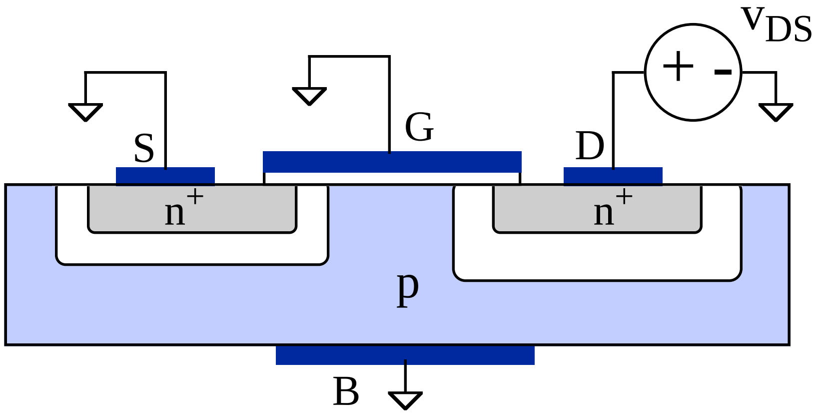


Enhancement Mode MOSFETs

- Depletion regions around the p-n junctions due to the built-in voltages
- With all of the voltages set to zero, the S-B-D connections form an NPN

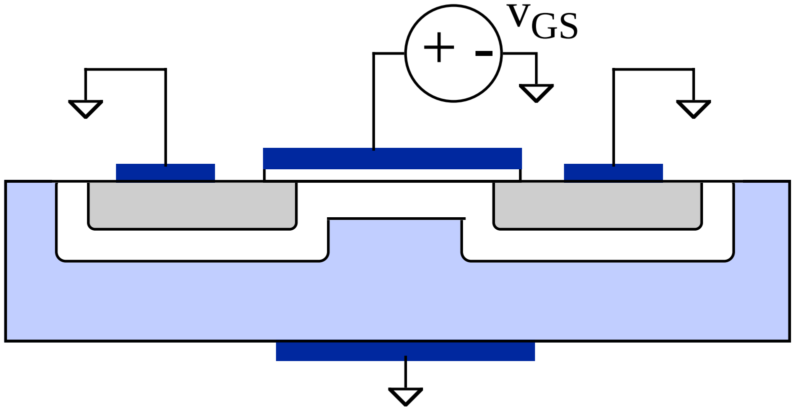


- Even with a postive drain voltage, there is no significant current flow



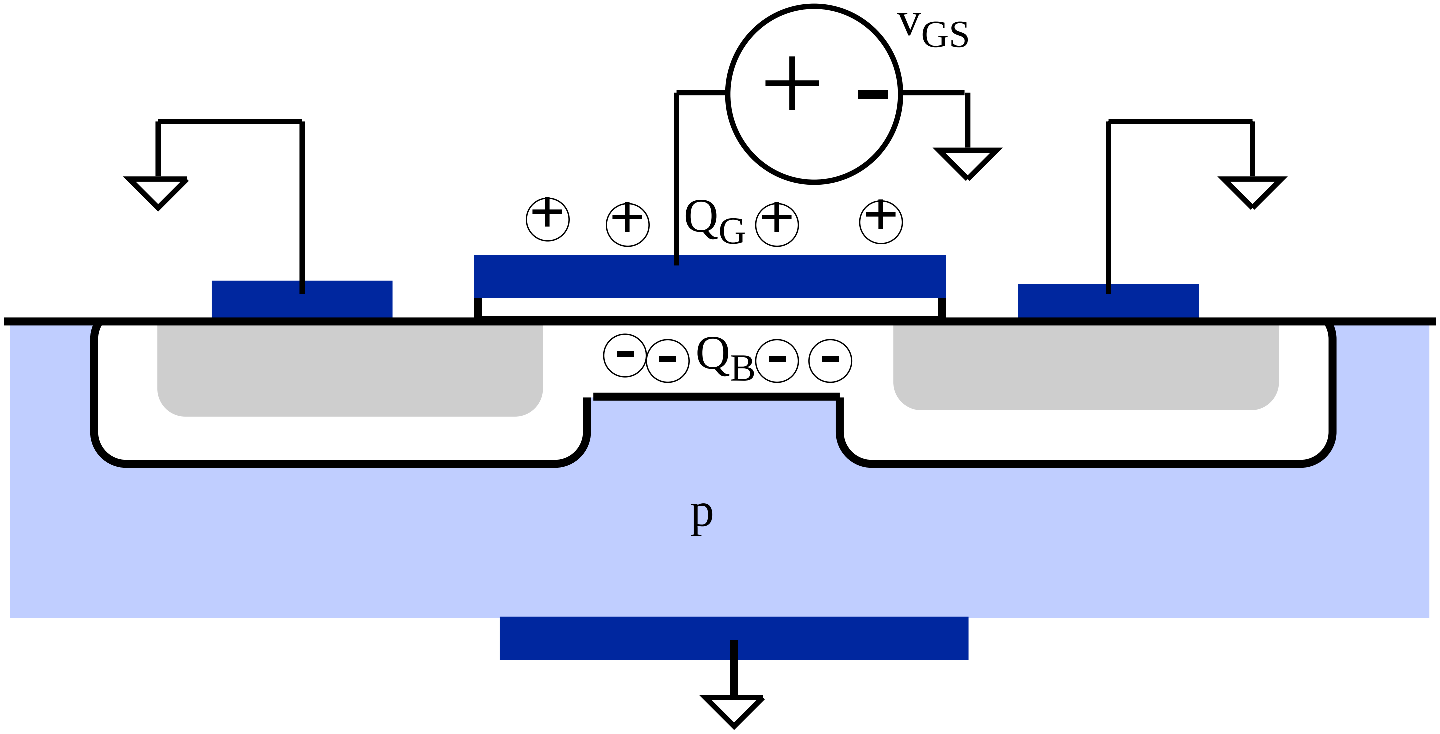
Enhancement Mode MOSFETs

- The gate is used to establish a connection between the source and drain nodes
- Postive gate voltage (for this NMOS enhancement transistor):
  - sets up an electric field from gate to bulk which tends to repel positive charges in the p-type bulk and create a depletion region
  - negative charge from the source and drain regions is attracted toward the channel by the same electric field



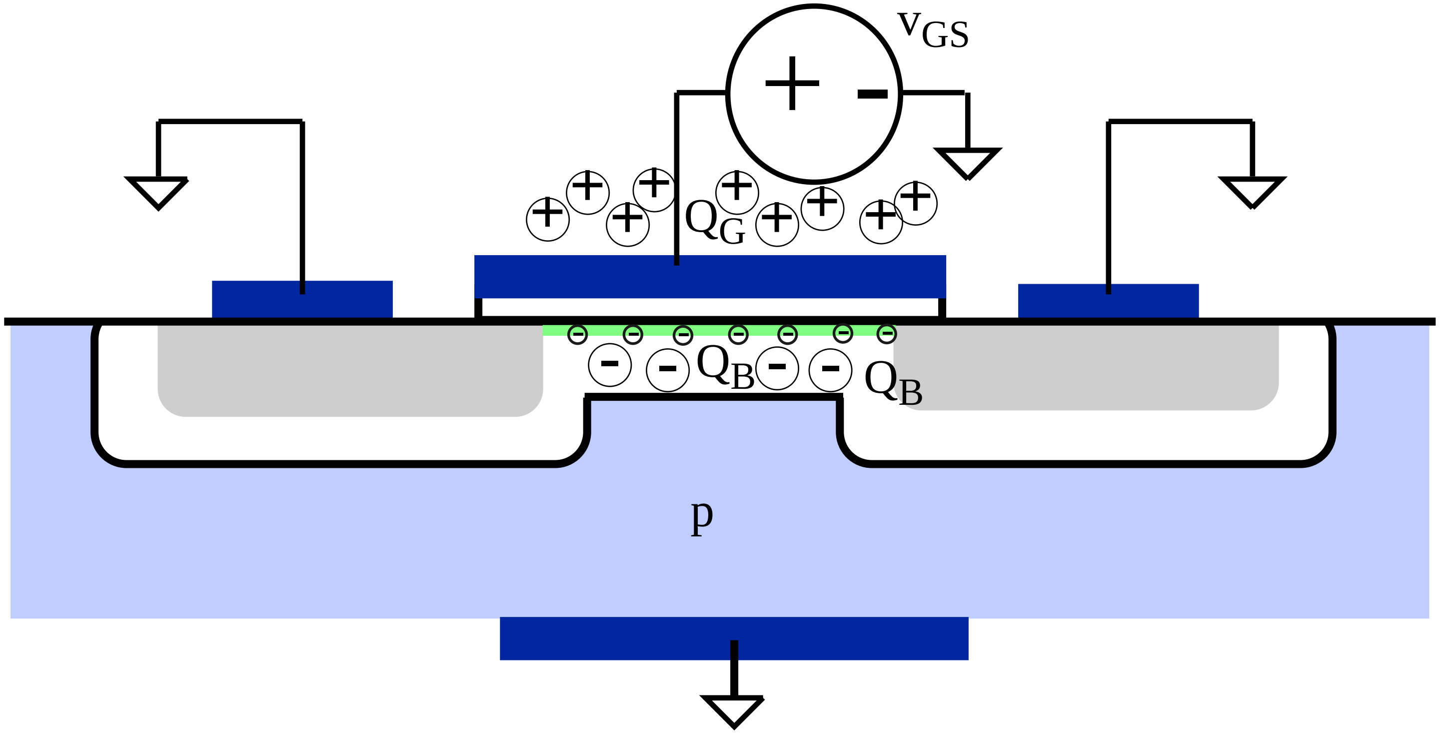
Enhancement Mode MOSFETs

- Gate to bulk acts like a capacitor



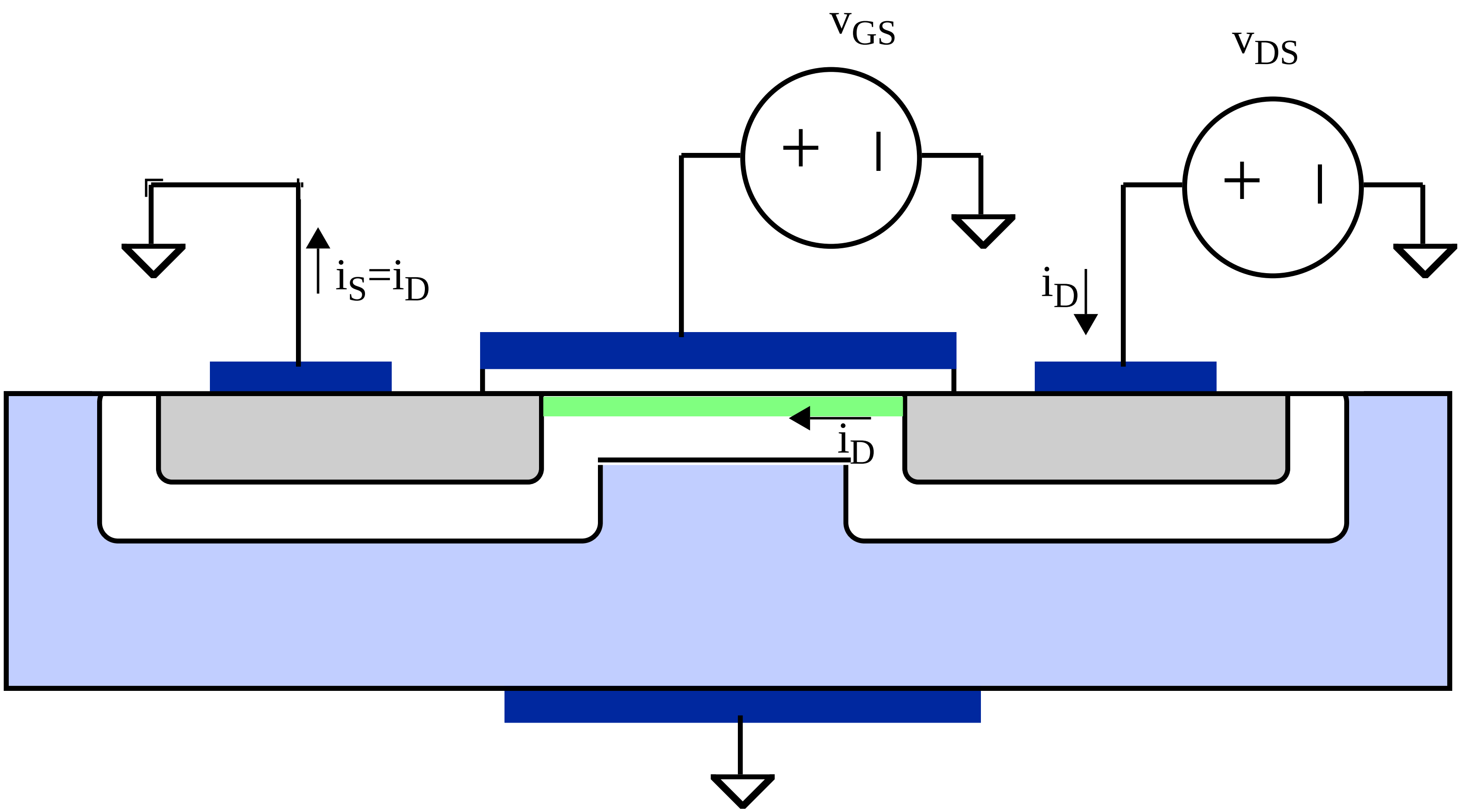
Inversion

- When the V_{GS} grows high enough, there is not enough holes at the surface to allow for electron recombination. Q_B becomes a negative fixed charge with density equal to $N_A$of the bulk.
- Additional gate voltage causes the free electrons to be drawn to the surface of the channel --- forming an inversion layer. When concentration of electrons at surface equals N_A we talk about strong inversion. Additional negative charge now comes from electrons in the channel.



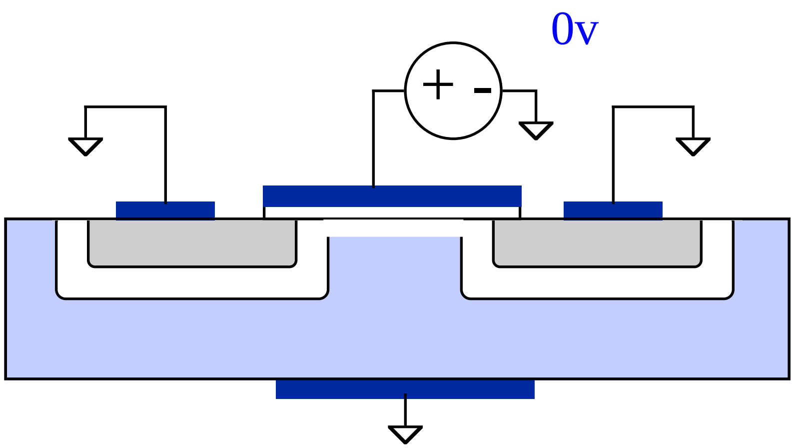
Threshold Voltage

- The gate voltage required to create strong inversion
- If there is a small potential difference between the drain and source, then a current will flow across the inversison layer which acts like a resistor

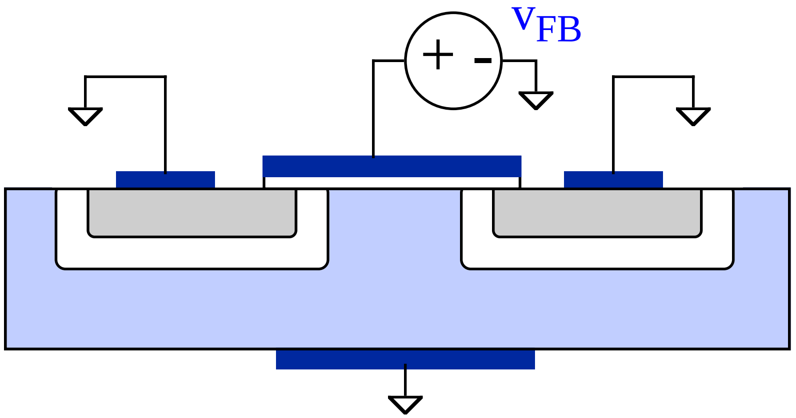


Flatband Voltage -- V_{FB}

- There is a depletion region (negative Q) under the channel even with $V_{GS} = 0$
  - Due to dangling bonds at the material interfaces and unwanted positive charges at the surfaces and in the oxides

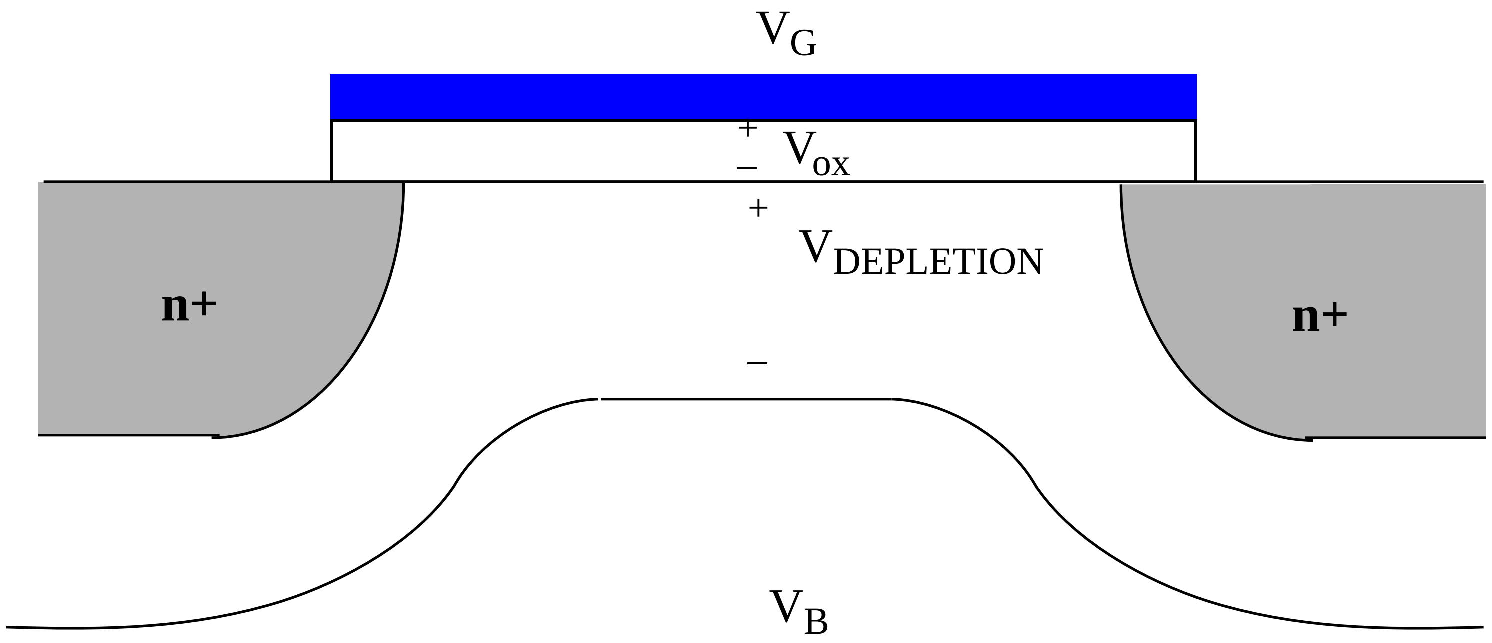


- The flatband voltage (generally negative) is the gate voltage required to exactly cancel this charge



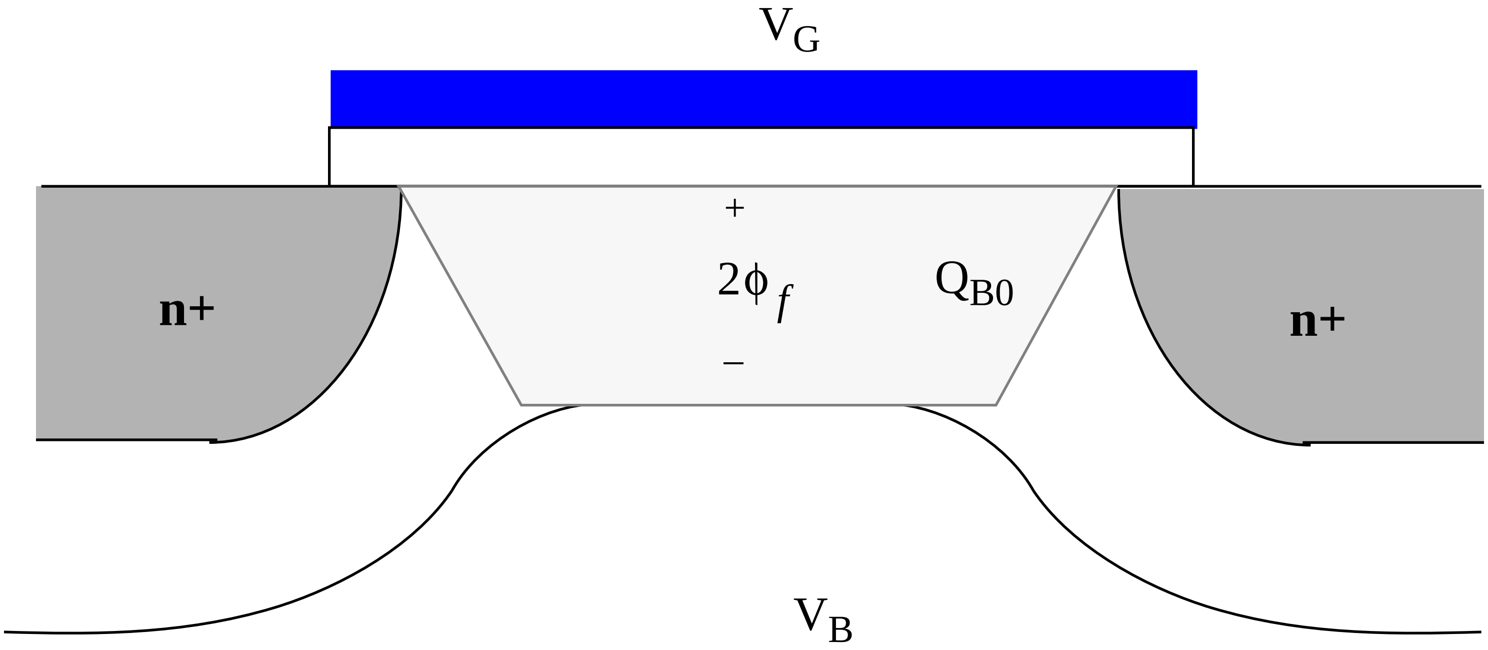
Threshold Voltage

- The threshold voltage is the flatband voltage plus whatever voltage is required to cause inversion in the channel



Threshold Voltage

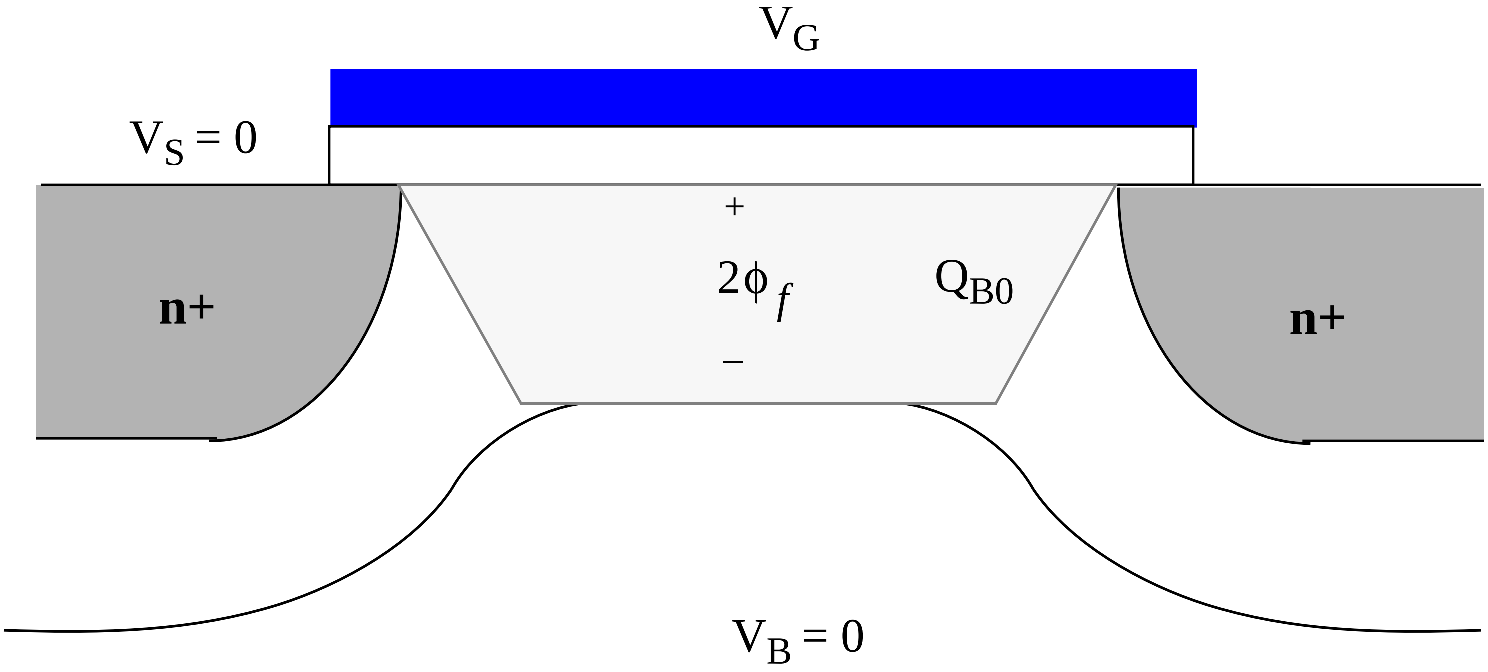
- Once -$Q_B = N_A$, then further increases in gate voltage brings about the inversion layer
- The depletion charge *and voltage* becomes fixed at a value called respecitively: Q_{B0} and $2\phi_f$
- Increases in channel charge correspond to the inversion layer charge, Q_I



Threshold Voltage

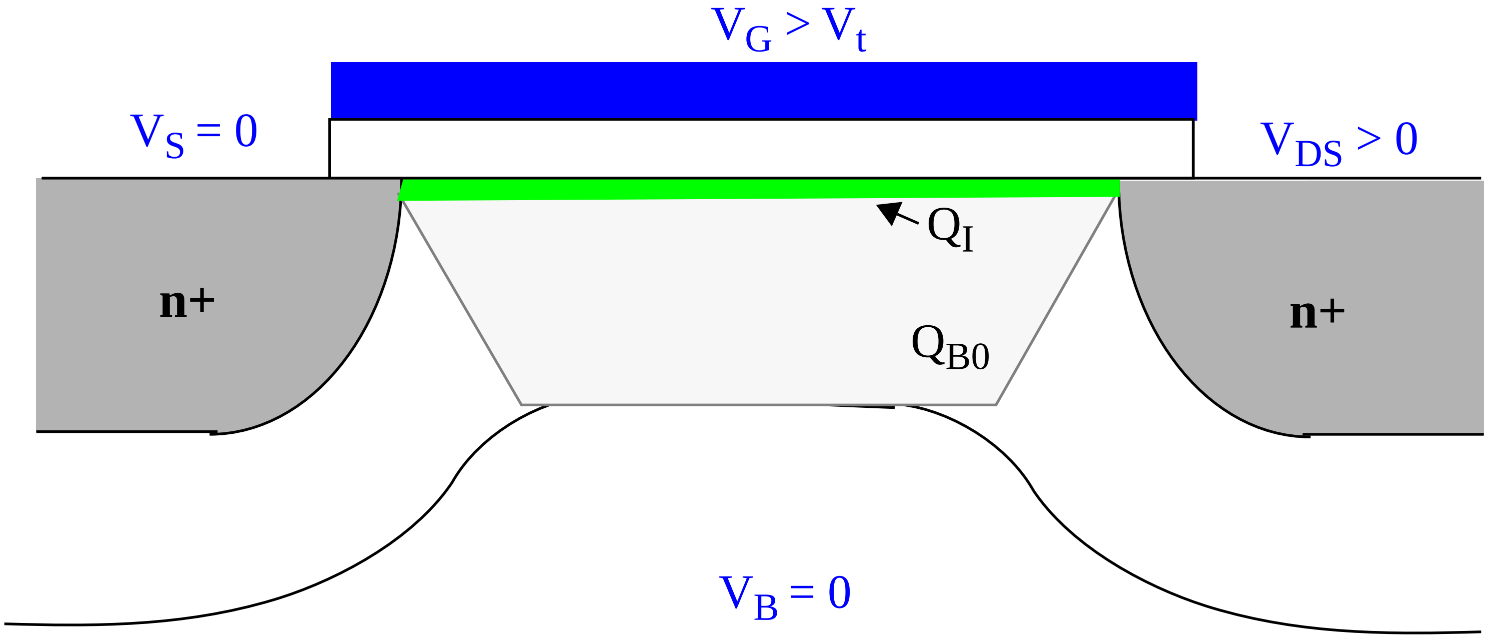
- Assuming V_B and V_S are both zero, the threshold voltage is:

$$V_{t0} = V_G\Big|_{threshold} = V_{OX} + V_{DEPL} + V_{FB}$$



Strong Inversion

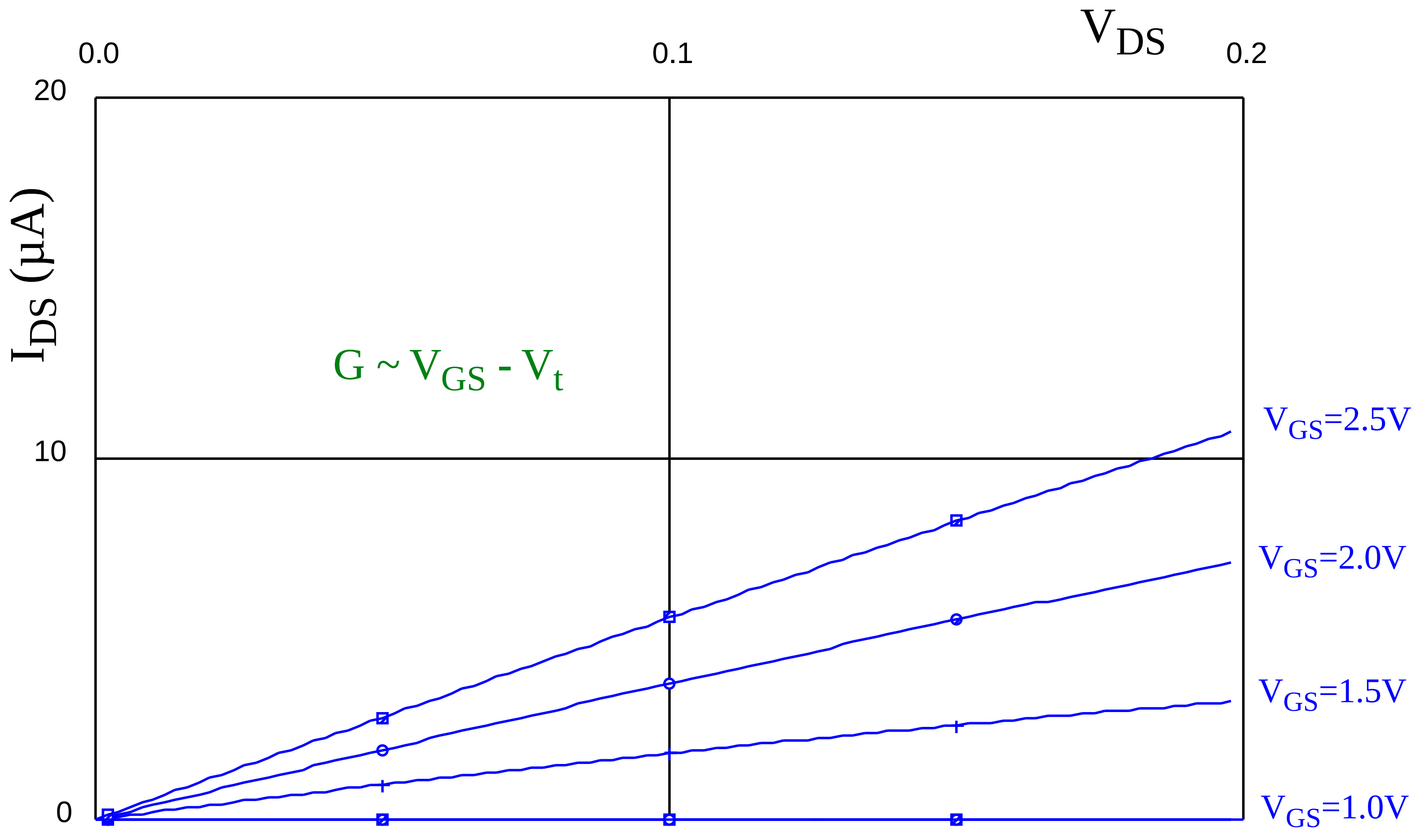
- With a small positive drain voltage, the inversion layer charge will drift from source to drain



- The conductance of the layer is proportional to $V_{GS} - V_t$

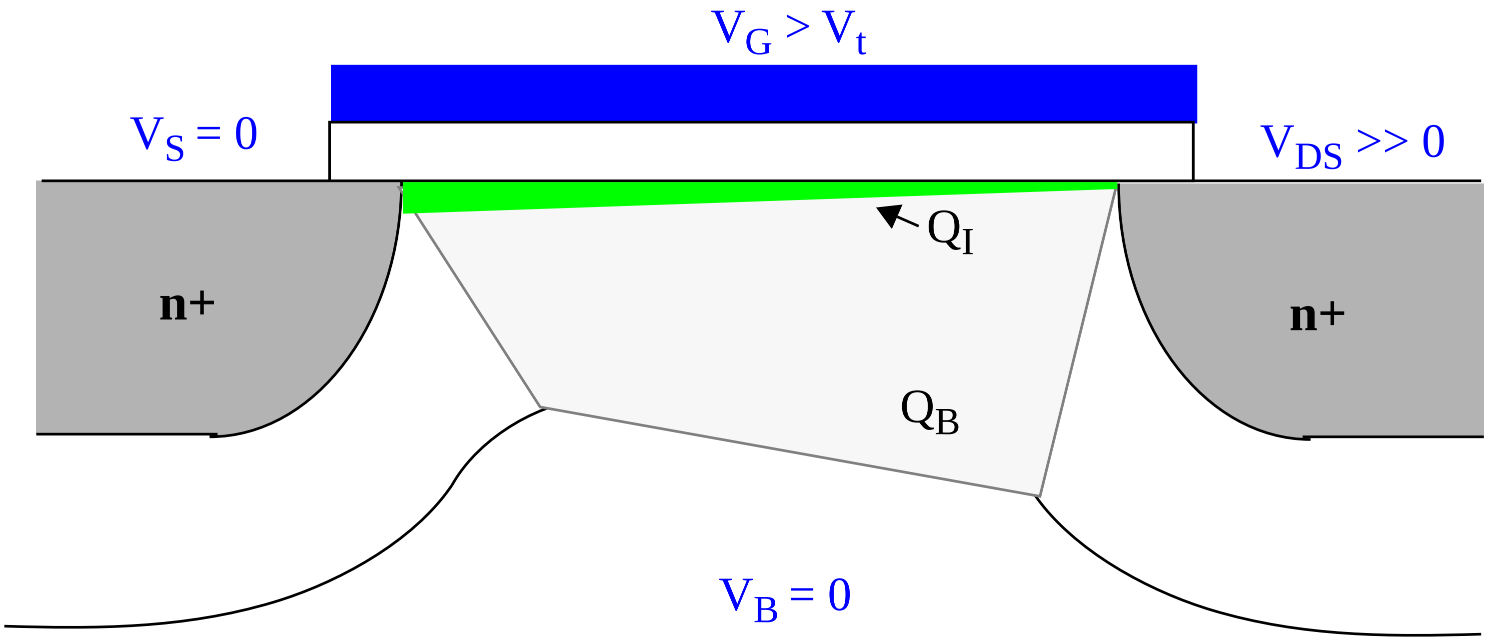
Inversion Layer Conductance

- Triode or linear region of operation
- Example: W=L=1 micron



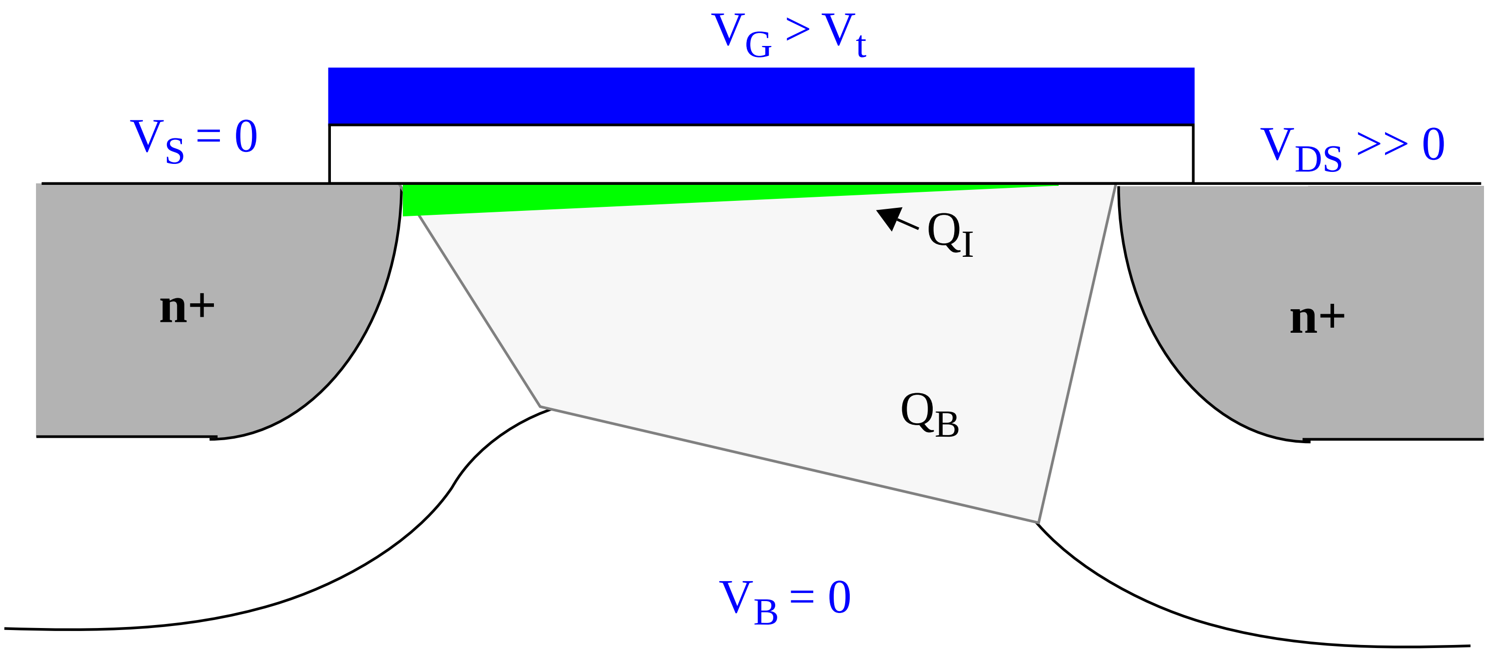
Pinch-Off Region --- Saturation

- The conductance is not always proportional to V_{GS}-V_t for all V_{DS}
- As V_{DS} increases, the bulk charge closer to the drain increases, and the inversion layer charge there decreases
- Conductance varies with position along the channel



Pinch-Off Region --- Saturation

- As V_{DS} increases further for a fixed V_{GS}, the inversion layer eventually goes to zero at the drain edge of the channel --- pinch-off

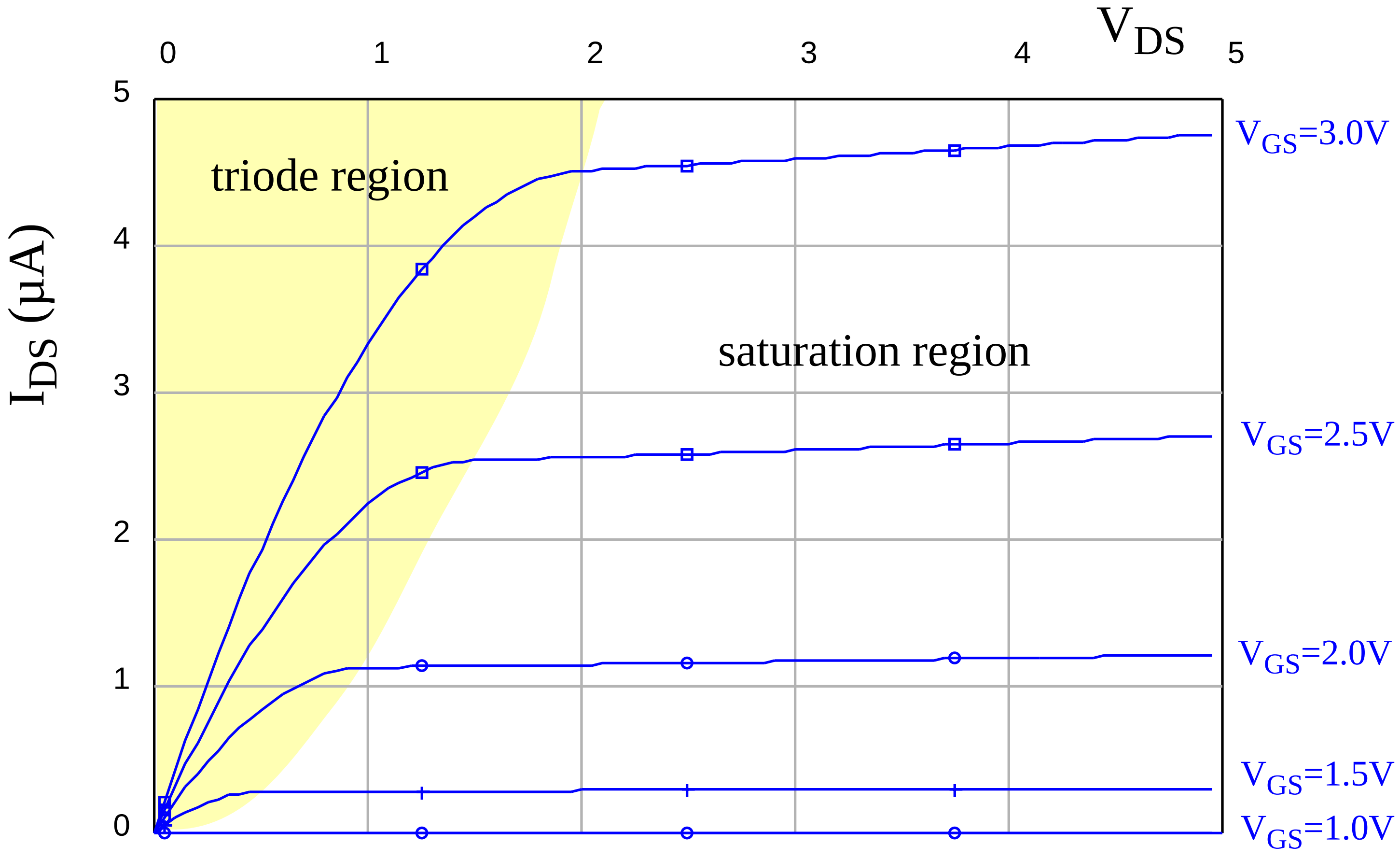


- Current is considered to saturate at this point since further increases in V_{DS} do not increase the current significantly

$$V_{DS}\Big|_{sat} \cong V_{GS} - V_t \qquad \text{why?}$$

Saturation Region

- Region of interest for analog design
- W=1 micron and L=10 microns



Here, staturation means “current saturation” which is different than “voltage saturation” in bipolar transistors

Equations

- Triode region equations for enhancement mode N-MOSFET

$$v_{GS} \geq V_t \qquad v_{DS} \leq v_{GS} - V_t$$

$$i_D = K[2(v_{GS} - V_t)v_{DS} - v_{DS}^2] \qquad K = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}$$

In SPICE: $K_n = \mu_n C_{ox} \quad \left[\frac{A}{V^2}\right]$

- For very small v_{DS}, as on page 15, what is r_{DS}?

Equations

- Saturation region equations for enhancement mode N-MOSFET

$$v_{GS} \geq V_t \qquad v_{DS} \geq v_{GS} - V_t$$

$$i_D = K[2(v_{GS} - V_t)v_{DS} - v_{DS}^2]$$

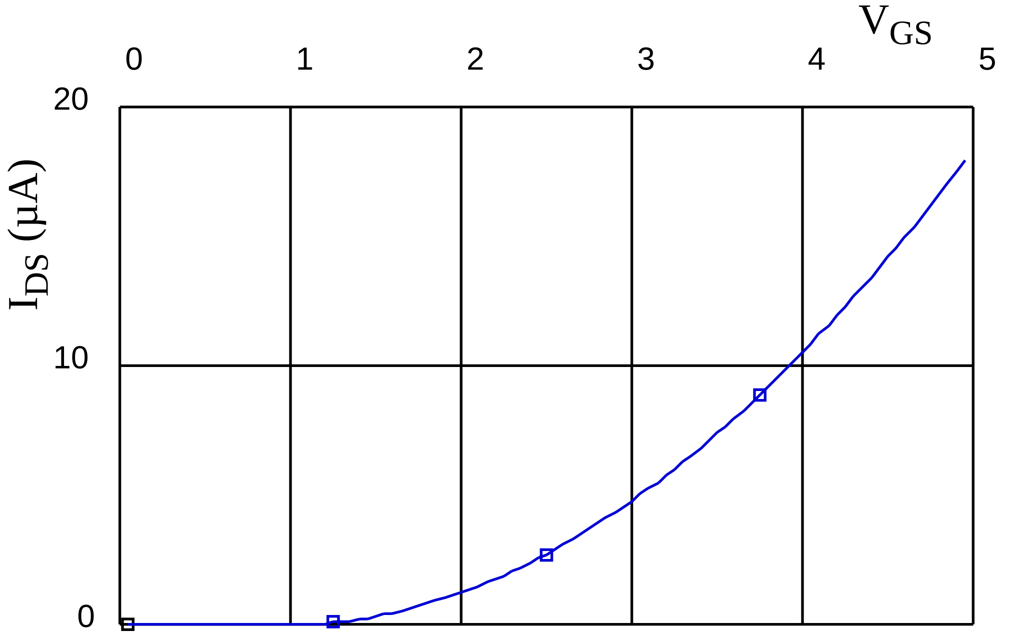
$$v_{DS}\big|_{sat} = v_{GS} - V_t$$

$$i_D = K[(v_{GS} - V_t)]^2 \qquad K = \frac{W}{2L}K_n \qquad K_n = C_{ox}\mu_n$$

- Current varies quadratically with v_{GS}

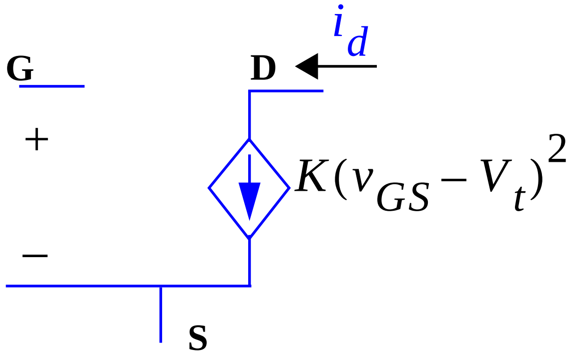
Saturation

- For $v_{DS} \ge v_{GS} - V_t$



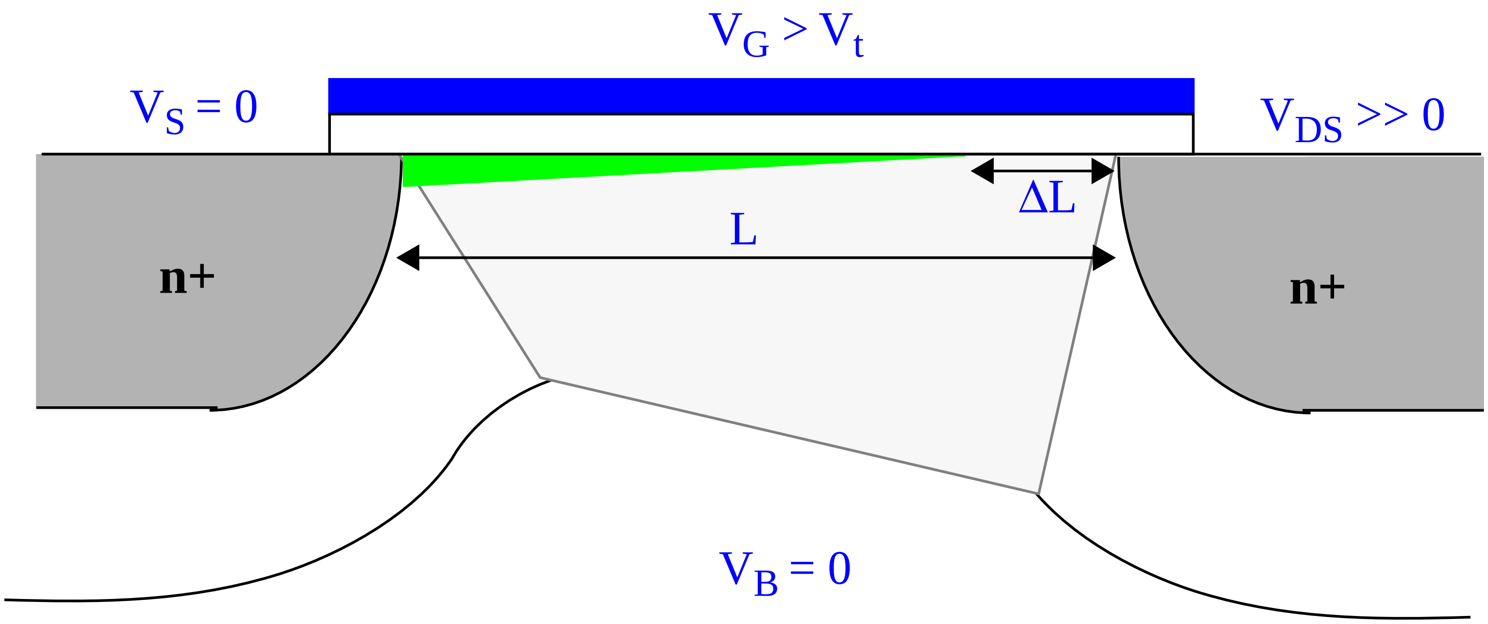
W=1 micron
L=10 microns
V_{t0}= 1 volt
K_n=2e-5 (A/v ^{2})

- Large signal model in saturation



Saturation --- Channel Length Modulation

- V_{DS} at the edge of the inversion layer remains fixed at V_{GS}-V_t
- But the effective length of the channel decreases with increasing V_{DS}
- Especially a factor when channel length is short



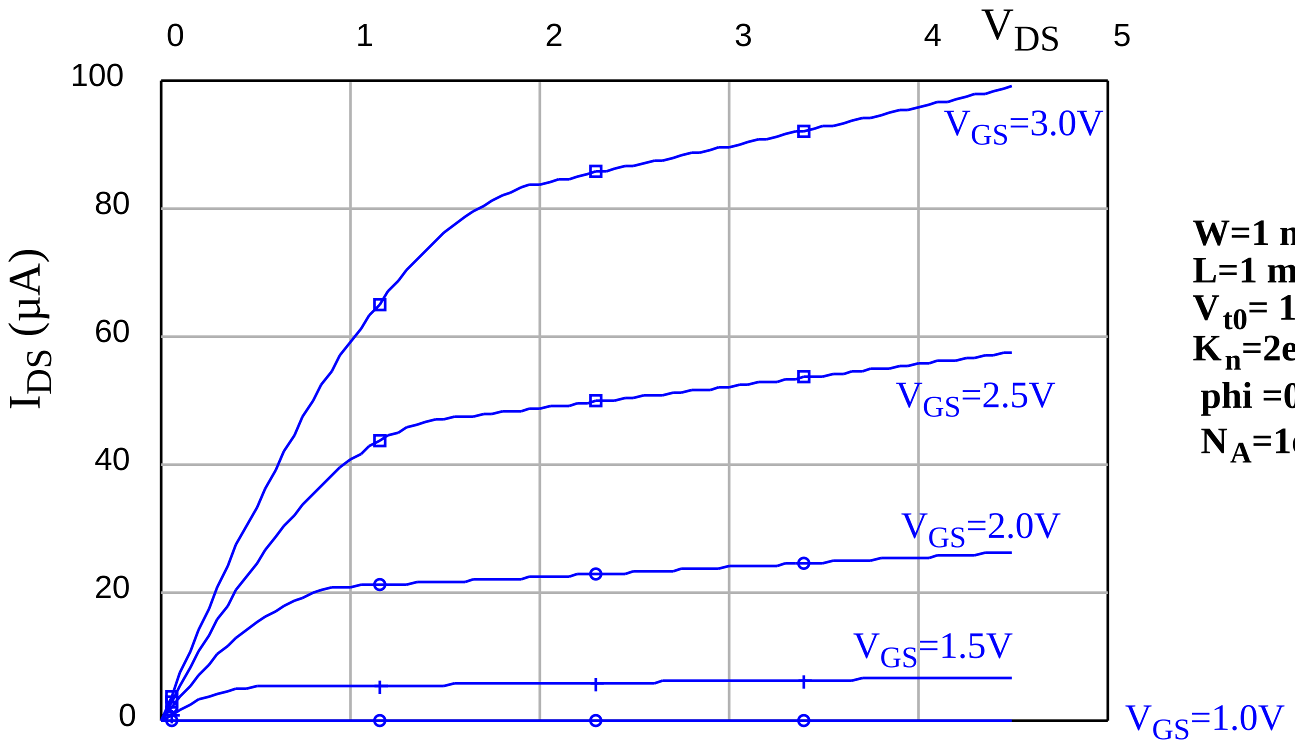
$$i_D\big|_{sat} = \frac{K_n W}{2(L - \Delta L)}[(v_{GS} - V_t)^2]$$

Saturation --- Channel Length Modulation

- Sometimes expressed in terms of channel length modulation parameter

$$i_D\Big|_{sat} = \frac{K_n W}{2L}[(v_{GS} - V_t)^2](1 + \lambda v_{DS})$$

- SPICE can calculate the modulation for you...

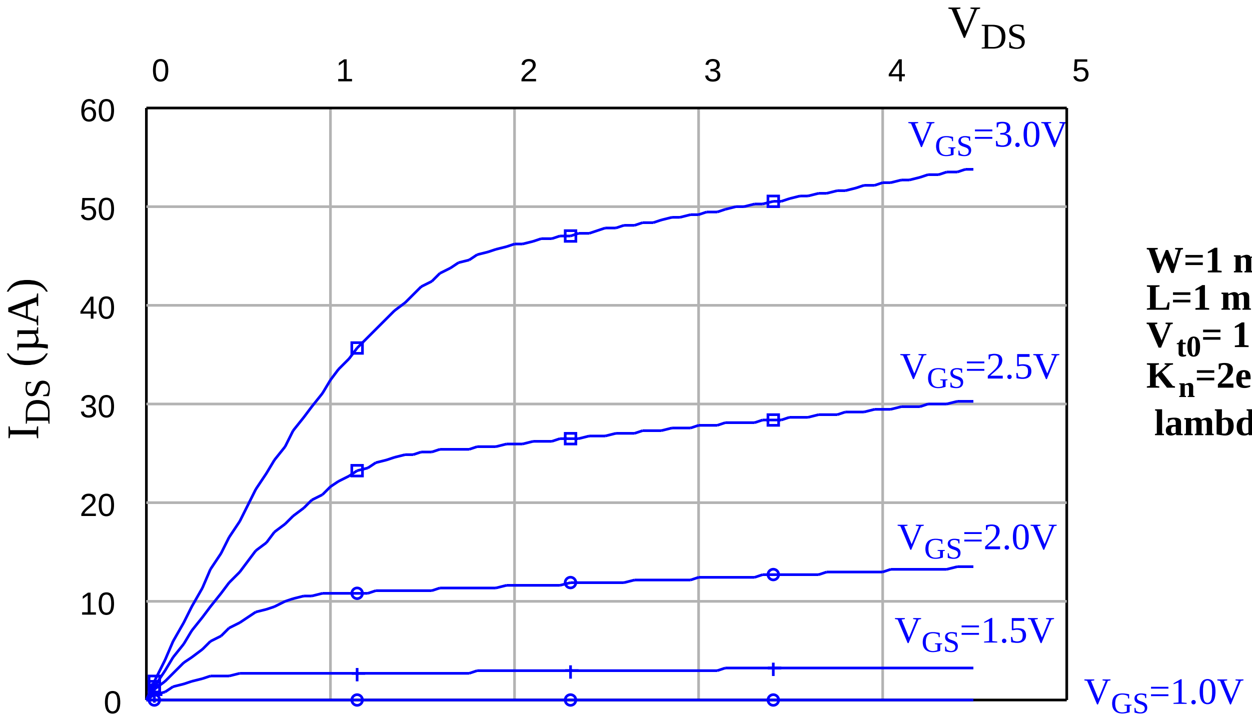


W=1 micron
L=1 microns
V_{t0}= 1 volt
K_n=2e-5 (A/v ^{2})
phi =0.6
N_A=1e15

Saturation --- Channel Length Modulation

- Or we can specify lambda explicitly in the model

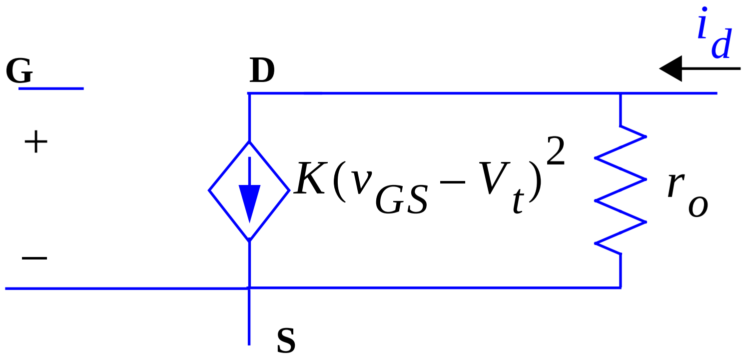
$$i_D\Big|_{sat} = \frac{K_n W}{2L}[(v_{GS}-V_t)^2](1+\lambda v_{DS})$$



W=1 micron
L=1 microns
V_{t0}= 1 volt
K_n=2e-5 (A/v ^{2})
lambda = 0.8

Output Resistance

- We can add a resistor to model the channel length modulation effect for the large-signal model in saturation



- What is the value of r_o?

$$r_o = \left(\frac{\partial i_{DS}}{\partial v_{DS}}\right)^{-1} = \left[\lambda K_n \frac{W}{2L}(V_{GS} - V_t)^2\right]^{-1} \approx \frac{1}{\lambda I_{Dsat}}$$