Texccelerate

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Project start: **Wed, 1/29/2025**

Display week: **1**

TASK	ASSIGNED TO	PROGRESS	START	END
Project Planning				
Decide on FPGA	Amelia, Andrew, Aniruidh	80%	1/29/25	2/5/25
Decide UI/UX Structure	Aniruidh, Amelia	100%	2/5/25	2/7/25
Decide Benchmark Softcores	Amelia, Andrew, Aniruidh	100%	1/29/25	2/12/25
Choose Target Model	Aniruidh, Amelia	100%	1/29/25	2/3/25
ML Model				
Test existing BitNet Model	Amelia, Andrew, Aniruidh	100%	1/29/25	2/1/25
Select Text model for quantize	Aniruidh, Amelia	100%	1/31/25	2/5/25
Quantize text model	Aniruidh, Amelia	100%	2/5/25	2/19/25
Modify inference code for CPU soft core deployment	Aniruidh	100%	2/20/25	2/27/25
Modify inference code for FPGA deployment	Amelia	0%	2/28/25	3/14/25
FPGA Acceleration				
Implement Unified Performance Counter	Andrew	0%	2/19/25	2/26/25
Synthesize CPU/GPU soft cores	Andrew	0%	2/19/25	2/26/25
Decide FPGA Architecture + RTL	Amelia, Andrew, Aniruidh	0%	2/23/25	3/9/25
Verify Texccelerate RTL	Andrew, Amelia	0%	3/10/25	3/17/25
Synthesize Texccelerate on FPGA	Andrew	0%	3/18/25	4/1/25
Synthesize all system on FPGA	Andrew, Amelia, Aniruidh	0%	4/2/25	4/16/25
FPGA Interface, UI/UX				
Boot Linux on FPGA hard core	Aniruidh, Amelia	0%	2/28/25	3/3/25
FPGA to computer SSH framework	Amelia	0%	3/3/25	3/13/25
FPGA PS to PL communication framework	Andrew	0%	3/14/25	3/24/25
Stream PMU metris through SSH	Aniruidh	0%	3/25/25	4/1/25
UI/UX Software Interface	Aniruidh, Amelia	100%	2/10/25	2/24/25
Whole System Integrated testing	Andrew, Aniruidh, Amelia	0%	4/2/25	4/16/25