

The Bluetooth Audio Rejiggering Instrument (B.A.R.I.)

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Abstract— Most audio effects pedals are unable to interface with common Bluetooth speakers. In this paper, we present BARI, a 4-channel Bluetooth audio effects pedal aimed toward the casual/hobbyist musician market. BARI allows anyone to apply digital and true analog effects to up to four instruments or vocal channels and perform with any Bluetooth speaker.

Index Terms— audio effects, audio effects pedal, Bluetooth, Bluetooth speaker, distortion effect, overdrive effect

1 INTRODUCTION

Audio effects pedals are devices widely used by musicians to add "effects" such as distortion, reverberation, or equalization to the signals produced by their instruments. However, these pedals are typically costly and must be wired to bulky professional power amplifiers and speakers. Our product, the Bluetooth Audio Rejiggering Instrument, provides an inexpensive alternative for casual performers. BARI is a 4-channel bluetooth audio effects pedal: it can apply a mix of digital and true analog effects that are competitive with desirable pedals. Unlike these pedals, it also broadcasts an output signal over Bluetooth, allowing high versatility as it can be used with cheap and extremely portable Bluetooth speakers.

In order for BARI to be an effective all-in-one solution for our target customers, it must be portable (maximum dimension < 15 cm, battery operated with a lifetime of at least 4 hours under standard operating conditions at room temperature), it must be inexpensive ($< \$100$ fabrication cost at production pricing), and it must provide a set of minimum audio effects which include an analog overdrive effect and basic delay, chorus, and EQ effects implemented digitally. It must also pair with all common Bluetooth speakers with a pairing range exceeding two meters. Further requirements are developed in the next section.

2 DESIGN REQUIREMENTS

2.1 Requirements and Justification

Design requirements for BARI are derived from our expectations about reasonable use of our device by casual musicians. The first five system requirements outline basic requirements for making the system usable by our intended

customer, which are outlined in the introduction: S.R. 1 - TEMPERATURE: The system shall meet all of the following requirements at room temperature ($+27$ C).

S.R. 2 - SYSTEM FORM FACTOR: To ensure portability, the system shall weigh less than 5 kilograms and its maximum dimension shall be less than 15 cm.

S.R. 3 - SYSTEM COST: The estimated production cost for the system at a volume of 10,000 units shall not exceed \$100, where this estimate is calculated by the sum of: (a) Quoted PCB manufacturing cost for 10,000 units. (b) Component cost estimated at 10,000 unit volume pricing. (c) Estimated cost for the mechanical enclosure at 10,000 units.

S.R. 4 - BATTERY LIFETIME: The system shall be capable of operating on battery power for at least 4 hours of continuous operation at Standard Operating Profile.

S.R. 5 - SYSTEM VOLTAGE SUPPLY: The system shall be capable of recharging from a 5VDC supply provided by a standard USB-C connector.

The following three system requirements define the input to our system. These are based on our research regarding common signal and impedance characteristics for input devices (microphones, instruments) which may be used by our target customers:

S.R. 6 - INPUT CONNECTOR DEFINITION: The system shall have 4 audio input channels through hybrid connectors that will accept XLR (standard microphone) or 1/4" (standard electric guitar) plugs.

S.R. 7 - INPUT SIGNAL DEFINITION: The system should be capable of accepting any audio-frequency (20~20 kHz) signal, with impedance from 100 to 40,000 ohms and magnitude from -60 dBV to +1.78 dBV, balanced or unbalanced. In particular, the system shall be capable of accepting the following common use cases: (a) "Quiet Mic": -59 dBV, ZOUT < 500 ohms, balanced; (b) "Hot Mic": -32 dBV, ZOUT < 500 ohms, balanced; and (c) Instrument: -59 dBV (passive) ~ 1.78 dBV (active, line-level), ZOUT = 10 ~ 40 kohms, unbalanced.

S.R. 8 - INPUT IMPEDANCE: The pre-amplifier's input impedance shall be: (a) Balanced, and (b) At least ten times the impedance of the highest-impedance allowed input.

The following three system requirements are flowed down requirements for the pre-amplifier block. In order for the system as a whole to exhibit high audio quality, the user's audio signals must experience low distortion during pre-amplification and arrive at the ADC interface with sufficient amplitude to achieve good SQNR.

S.R. 9 - PRE-AMPLIFIER OUTPUT: For each of the input the pre-amplifier shall produce an output voltage which is: Single-ended, referenced to the VSS supply of the system, and Tunable from -20 dBFS to -2 dBFS, where FS refers to the Full Scale of the microcontroller ADC (Approximately 3.3V)

S.R. 10 - PRE-AMPLIFIER GAIN FLATNESS: The gain of the pre-amplifier block shall differ by no more than 2 dB from its average value across the passband (20~20 kHz)

S.R. 11 - PRE-AMPLIFIER DISTORTION: The pre-amplifier shall introduce total harmonic distortion not exceeding -60 dB(carrier) as approximated by the sum of the second and third harmonics of a test tone.

Because any analog distortion effect will intentionally create noise on the signal, traditional metrics are not applicable. We opted to validate our analog effect through a comparison with a SPICE model of a prestigious existing pedal (the Colorsound Overdriver) which serves as our model.

S.R. 12 - ANALOG OVERDRIVE PERFORMANCE: When activated, the Analog Effect circuit shall process its input to create a distorted output waveform that is similar to the output of the simulated Reference Overdrive Pedal, except that the input and output signals will be smaller in magnitude by a factor proportional to the difference in supply voltage between the two designs. In particular:

(a) For a pure tone with identical input amplitude and an identical gain setting, the Analog Effect shall produce a soft-clipped waveform with magnitude within 10 dB of that of the Reference Overdrive Pedal, and

(b) The 2nd and 3rd harmonics of the tone shall be no more than 5 dB less than those produced by the Reference Overdrive Pedal.

(c) For identical tone control and gain settings, the Analog Effect shall produce a frequency characteristic that is within 10 dB of that produced by the Reference Overdrive Pedal over the frequency range of interest (20~20 kHz).

The defining feature of BARI is its Bluetooth capability. The following two system requirements define the range and connection protocol our Bluetooth module must support to be viable:

S.R. 13 - BLUETOOTH TRANSMISSION PROTOCOL: The system shall support the following Bluetooth specifications for audio transmission: (a) Bluetooth pairing to at least one Bluetooth audio output device, (b) Bluetooth version 3.0 or higher, (c) Low-Complexity Subband (SBC), Advanced Audio Coding (AAC), or other common codecs, capable of at least 250kbps, (d) Advanced Audio Distribution Profile (A2DP) Bluetooth profile.

S.R. 14 - BLUETOOTH TRANSMISSION RANGE: The average distance at which the system can maintain connection to a standard bluetooth speaker in an open air environment shall exceed 2 meters.

The following system requirements describe the digital

effects that we must provide for a minimum viable product as well as metrics for the quality of each of these effects, as well as the overall latency of the digital processing. These figures are derived subjectively with advice from Sam Rainey regarding sound quality.

S.R. 15 - MINIMUM DIGITAL EFFECTS: The system shall be capable of applying any of the following digital effects (non-concurrently) to any of the four input channels independently, defined by the following requirements: (a) Equalization (EQ), (b) Delay, and (c) Chorus

S.R. 16 - EQUALIZATION QUALITY: For each equalization band in the system (at minimum, bass, middle, and treble), the system shall be able to adjust the magnitude of that band with a dynamic range of +/-20 dB, without affecting the amplitude in the non-adjusted bands by more than +/- 5 dB.

S.R. 17 - DELAY WET/DRY RATIO: The system shall be able to create a 0% wet delay output and a 100% wet delay output with 10 intermediate tuning steps.

S.R. 18 - DELAY TIME: The delay time shall be adjustable from 0 to 350 ms with 10 intermediate tuning steps.

S.R. 19 - CHORUS MODULATION DEPTH: The system shall provide a modulation depth of 0 to 5 ms with 10 intermediate tuning steps.

S.R. 20 - CHORUS RATE: The system shall provide a rate of 0 to 5 Hz with 10 intermediate tuning steps.

S.R. 21 - CHORUS WET/DRY RATIO: The system shall be able to create a 0% wet chorus output and a 100% wet chorus output with 10 intermediate tuning steps.

S.R. 22 - PROCESSING LATENCY: The system shall have end-to-end latency of < 100 ms from the system input to the Bluetooth send.

The final four system requirements determine both the form and the latency of our user interface, and they are defined to provide a responsive user experience:

S.R. 23 - USER INTERFACE RESPONSE LATENCY: The system shall finish responding to any user input (i.e. return feedback to the user) within 100 ms.

S.R. 24 - USER INTERFACE UPDATE LATENCY: When the user adjusts a parameter through the user interface, the system shall update its state (i.e. gain settings on analog circuitry and DSP parameters) within 1s.

S.R. 25 - USER INTERFACE INTERACTION TIME: The user shall be able to navigate to any command within 5s.

S.R. 26 - USER INTERFACE FEEDBACK MECHANISM: The system shall display a hierarchical menu in which the menu item that the user is currently interacting with is highlighted. The menu will contain: (a) All settings the user can adjust, and (b) The current system state.

2.2 Testing to Requirements

The requirements above are designed to be detailed enough that it should be fairly obvious how to verify them. However, to standardize the manner in which BARI is

tested and establish a regular format for recording results, we are currently developing *The BARI Test Procedure* (to be released), a document which describes ten functional tests for verifying the above requirements as well as a bringup procedure for the software. Please refer to Table 9 for a matrix of how our functional tests relate to the requirements above.

3 ARCHITECTURE OVERVIEW

The Bluetooth Audio Rejigging Instrument accepts audio input from up to four XLR / 1/4" hybrid jacks. It mixes and applies effects to these audio signals based on a user directives given via an LCD + rotary encoder user interface. BARI then broadcasts the resultant signal over Bluetooth. BARI is battery-operated, and it can be recharged via a standard USB-C jack. The system is fully programmable via JTAG.

BARI is integrated on a single printed circuit board which contains five distinct functional modules as seen in the block diagram (Fig. 1):

- The Pre-Amplifier Module
- The Analog Effect Module
- The Microcontroller Module
- The Bluetooth Module
- The User Interface Module
- The Power Module

The essential functions of each block and the interfaces between them are described below. By convention, an interface which is an output from module A to module B is listed under module A.

The Pre-Amplifier Module (4x) accepts balanced or unbalanced audio input signals (S.R. 7) and applies variable pre-ADC gain which is adjustable via an I2C-controlled digital potentiometer.

Interfaces:

- Analog audio output to Analog Effect Module or Microcontroller Module

The Analog Effect Module (2x) applies a variable amount of analog distortion to the Pre-Amplifier Module's output on the 2 of 4 channels for which it is available. For each of these channels, an analog multiplexer controls whether the output from the Pre-Amplifier Module is passed through the Analog Effect Module, or whether it is directly passed to the Microcontroller Module without distortion.

Interfaces:

- Analog audio output to Microcontroller Module

The Microcontroller Module contains the core STM32 microcontroller which controls all other modules via SPI, I2C, and UART as well as applying digital audio effects. The module also contains the 16-bit external ADCs which digitize output from the previous two modules and pass it to the STM32 via time-multiplexed SPI.

Interfaces:

- Time-Domain-Multiplexed SPI audio data from the external ADC to the microcontroller
- I2S audio output to the Bluetooth Module
- I2C control bus to the digital potentiometers in the Pre-Amplifier and Audio Effect Modules
- SPI control bus to the LCD in the User Interface Module
- UART control bus to the Bluetooth Module

The Bluetooth Module receives processed audio from the Microcontroller Module over Inter-Integrated Circuit Sound Bus (I2S) and broadcasts the signal as an output over Bluetooth.

Interfaces:

- Wireless audio output to an external Bluetooth speaker

The User Interface Module consists of an LCD screen and a rotary encoder with a push button, as well as a secondary foot switch. The LCD displays a menu structure with various options for the user while the rotary encoder allows the user to navigate the menus and make selections. The foot switch allows the user to quickly toggle on/off effects.

Interfaces:

- Gray code output from the rotary encoder to the Microcontroller Module
- Discrete digital output from the foot switch and push button to the Microcontroller Module

The Power Module consists of the 3.6V rechargeable battery that supplies all other modules with power and the USB-C power port that allows the battery to be recharged.

Interfaces:

- N/A

4 DESIGN TRADE STUDIES

4.1 Implementation Plan (Make vs. Buy)

As described in the Architecture Overview, BARI will be implemented on a custom printed circuit board. This means that the vast majority of the hardware will be implemented as a custom design using standard components

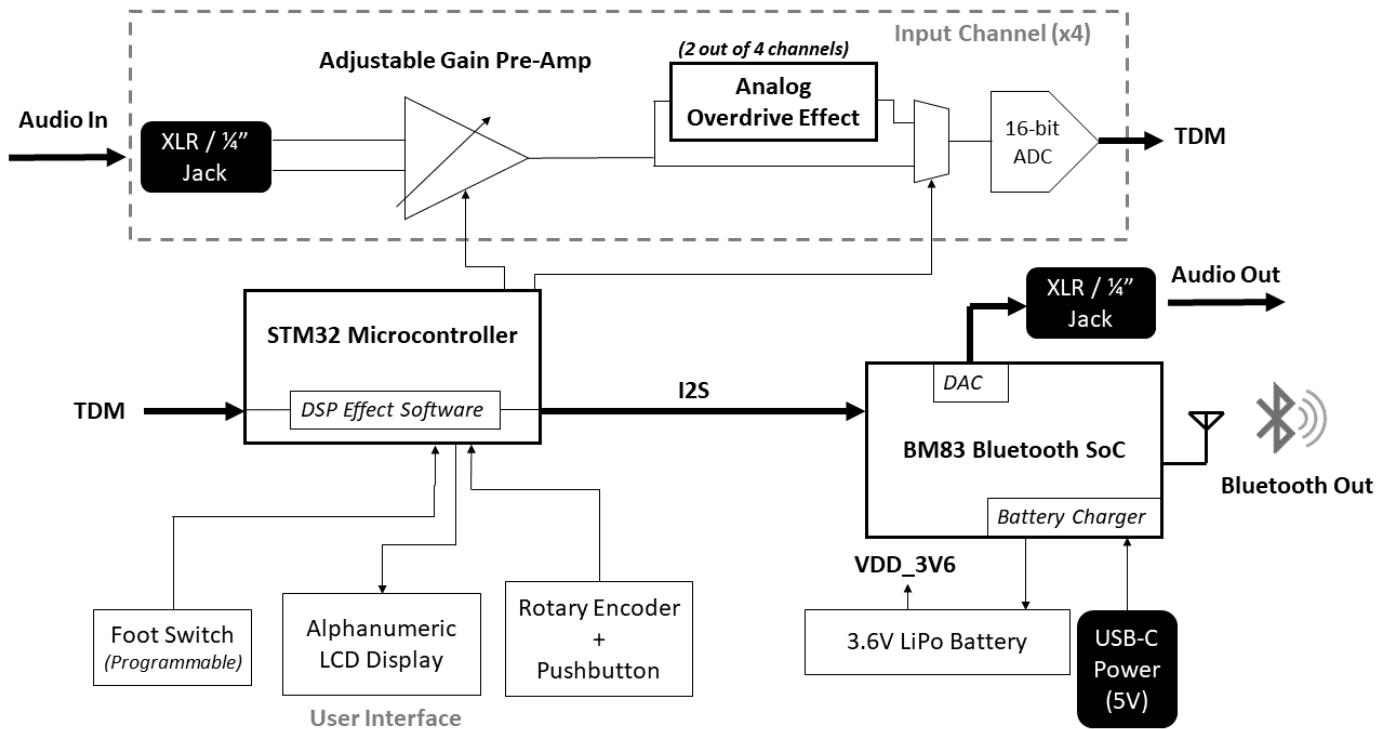


Figure 1: Bluetooth Audio Rejiggering Instrument (BARI) Block Diagram

purchased from Digikey. The notable exception is the Analog Effect Module, which is referenced to a specific legacy pedal design as described below.

Our software is a mixture of custom modules (in particular our DSP and system control code) with STM32 and BM83 library code. Fig. 6 illustrates which software components are library vs. custom code.

4.2 Pre-Amplifier Module

4.2.1 Design Specification

The pre-amplifier module is the first block in the BARI signal path, and its performance is critical to ensuring system signal integrity. Its key specifications include the capability of providing a large, tunable gain (-60 dBV to +1.78 dBV, or a dynamic range of 61.78 dBV, S.R. 7) while maintaining gain flatness of less than 2 dB (S.R. 10) and introducing harmonic distortion not exceeding -60 dB (S.R. 11). These numbers were derived from comparable specifications for professional audio equipment, and they are intended to prove good signal integrity. Additionally, the pre-amplifier must have low Size, Weight, and Power (SWaP) as it will be implemented four times (once per channel).

4.2.2 Trades and Design Choice

Many different digitally tunable gain topologies were considered from the pre-amplifier block, including programmable gain amplifiers (PGAs), instrumentation amplifiers and au-

dio amplifiers that are tunable via digital potentiometer, and multiplexed fixed gain blocks.

PGAs offer easy tuning, but they are not a good fit for the application: most of the inexpensive (<\$3.00) PGAs we examined had only single-ended or low-impedance inputs. One promising candidate (LT1996) was only pin-programmable and thus not well suited for a digitally re-programmable application.

Instrumentation Amplifiers offer excellent performance for very small input signals and balanced inputs (such as microphone signals), but they are less appropriate for large instrument-level signals. Many InAmps also have a minimum gain setting (5 V/V for the INA2332), which can cause clipping with our relatively low supply voltage.

Fixed gain blocks offer a wide dynamic range but very coarse tuning, which makes them at best only a partial solution to the problem.

We ultimately settled on a potentiometer-tunable audio-class amplifier, the MAX4061, which features balanced differential inputs, relatively low supply current (750 μ A), tunable gain from 0 to 40 dB, and excellent PSRR, CMRR, and THD+N characteristics. The one drawback of this choice was that the MAX4061 cannot meet our full required dynamic range. However, this was mitigated due to our choice of an ADC (the PCM1864) which includes over 30 dB of tunable analog gain. For the tuning potentiometer, we selected the MCP4451, which contains four potentiometers on a single chip that may be tuned easily using I2C.

For a full list of analog components that we considered, see smarturl.it/bari-analog-trades

4.3 Analog Effect Module

4.3.1 Design Specification

The primary specification for the analog effect module was to create a "desirable" analog distortion effect. For marketing and testability reasons, we decided to base our design on an existing analog effects pedal which could be simulated in SPICE to use as an objective comparison point (see S.R. 12).

4.3.2 Trades and Design Choice

The two primary effects we considered were analog delay and analog overdrive. We moved away from analog delay after learning that this effect is typically implemented with a "Bucket Brigade Device" (BBD) chip which is difficult to procure.

Our primary source for overdrive effects was the compilation of hobbyist schematics at <http://beavisaudio.com>. From the effects listed there, we downselected to the Colorsound Overdriver effect due to its versatility, with the ability to produce a range of gain from light overdrive to heavy distortion and even fuzz. Other factors include its subjective "coolness" and the fact that it could be implemented with a relatively small number of components. We were also able to find detailed factory schematics for the original Colorsound Overdriver pedal, confirming this trade.

For a full list of analog components that we considered, see smarturl.it/bari-analog-trades

4.4 Microcontroller

4.4.1 Design specification

The microcontroller should have a supply voltage that is roughly in the range of common batteries and USB-C wall adapters, and better if it has low power consumption, so that the system can be portable and easy to charge. It should have an ADC of at least 16-bits to support high music signal quality, and support DSP instructions in order to execute the digital effects quickly and efficiently. It should also support the LCD interface and common communication protocols like I2C, SPI, I2S to interface with all other modules. ARM core is preferred due to good programability and our familiarity with it. It should have low cost and have an affordable launchpad / discovery kit with peripherals similar to what we will actually have on our hardware to facilitate testing.

4.4.2 Trades and design choice

Table 1 shows the tradeoffs between 4 microcontroller options. The cost refers to the launchpad cost, which we will purchase for testing before our custom PCB arrives. The voltage for all 4 microcontrollers are 3.3V and thus

the current (active/idle) indicates the power consumption level.

Our choice is the STM32F407VG microcontroller with external ADC PCM1864DBTR. The boards with built-in 16-bit ADCs are usually high performance and have high power cost as well as monetary cost, so we choose to use another external ADC instead. The STM32L496AG and STM32L4S5VIT6 are low power, and also have useful peripherals like the LCD or Bluetooth module on its launchpad, which is convenient for early-stage testing, but the price of the launchpad is too high comparing to the first option, and our power budget and schedule indicates that we would not require such low power and we would receive our first test PCB board with all necessary peripherals on it soon after we start implementing.

4.5 Bluetooth Module

4.5.1 Design Specification

This subsystem is used for receiving the combination of all four of the processed inputs and transmitting the output signal to a host Bluetooth audio device (S.R. 13(a)).

The transmission must support Bluetooth 3.0 or a more recent version of Bluetooth (S.R. 13(b)) for sufficient range, data rate, and reliability. The module must offer A2DP as the Bluetooth profile (S.R. 13(d)), which is the universal profile for audio information. The module must be compatible with either the SBC codec, which is supported by any output device that uses A2DP, or the AAC codec, which is the default codec for Apple devices (S.R. 13(c)).

This subsystem must be powered by our system voltage supply of 3.3V.

4.5.2 Trades and Design Choice

BlueCreation's BC127 is a Bluetooth module that features Bluetooth 4.0 with support for the low-latency aptX codec as well as the standard AAC and SBC codecs. However, there is poor documentation, hindering the ease of use. Each unit costs around \$27.

Roving Network's RN-52 features Bluetooth 3.0 and supports the SBC codec. Like the BC127, there is little documentation. Each unit costs around \$25.

Microchip's BM83 features Bluetooth 5.0 and supports the AAC and SBC codecs. There is ample usage documentation provided and there is an included feature for pairing two Bluetooth audio devices simultaneously called Wireless Concert Technology (WCT). Each unit costs around \$11.

Refer to Table 2 for a chart comparing these modules.

The BM83 was selected for its excellent included documentation, low cost, and additional features including Bluetooth 5.0 and WCT.

uC	Core	Cost	Current	ADC	DSP	Memory	Audio	Other feature
STM32F407VGT6	M4 + FPU	\$20	40mA/0.3mA	12-bit (3)	Y	1M + 196K	I2S (2)	
STM32L496AG	M4 + FPU	\$70	7mA/2.8uA	12-bit (3)	Y	1M + 320K	SAI (2)	LCD on launchpad
STM32L4S5VIT6	M4 + FPU	\$54	13mA/2.8uA	12-bit (1)	Y	2M + 640K	SAI (3)	BT on launchpad
STM32H745XI	M7 + M4	\$87	(dual core)	16-bit (3)	Y	2M + 1M	SAI (4)	LCD on launchpad

Table 1: Microcontroller Trades

Module	Cost	Version	Codec(s)
BC127	\$27	Bluetooth 4.0	AAC SBC aptX
RN52	\$25	Bluetooth 3.0	SBC
BM83	\$11	Bluetooth 5.0	AAC SBC

Table 2: Bluetooth Module Trades

4.6 User Interface Module

4.6.1 Design Specification

This subsystem includes inputs that a user can adjust to tune, toggle, or alter the system state as well outputs that clearly provide a user with information about the system.

The user interface (UI) module must meet ease of use requirements regarding latency, the display, and time to make adjustments. Any change to an effect parameter must be perceivable within 1 second of the change (S.R. 25). A user must be able to apply changes or toggle effects on any channel within 5 seconds (S.R. 24). Further, the UI must be no more than 5 menu layers deep. A typical menu layer interface is channel select, effect select, effect parameter select, and effect parameter adjustment. The display should be at least 30mm wide by 10mm tall and offer a resolution of at least 128x32 pixels for sufficient visibility. A back-light for the display is preferable but not essential.

The UI module must meet control resolution requirements in order to support fine-tuned control of effects parameters. A user must be able to apply different effects for each individual channel. Tuning of effects parameters must be possible as outlined in the system requirements. The user must have the ability to apply or disable each effect on a channel.

This subsystem must be powered by our system voltage supply of 3.3V.

In order to maximize tunability of effects for each channel, avoid cluttered buttons, and allow for flexible firmware updates, the UI module must include a screen display of some sort. Liquid-crystal display (LCD) screens are a good choice due to their availability, low price, and compatibility with microcontrollers.

A touchscreen thin-film-transistor (TFT) LCD would not provide ease of use when tuning effects parameters due to the accuracy expected of the user when adjusting parameters by small amounts. In addition, they are more expensive and consume more power than a standard LCD.

The best option for tuning resolution is a rotating dial

so that a user has precise control. In addition, instead of a touchscreen interface, a button could be used to enter a selection. An option that combines these two features is the rotary encoder with a pushbutton.

A system power switch and a programmable footswitch are UI components that are not specified in the MVP, but would be helpful for a user.

The trade study will focus on different LCD screens and rotary encoders with a pushbutton.

4.6.2 Trades and Design Choice

4.6.2.1 LCD

Newhaven Display's NHD-C12832A1Z-FSB-FBW-3V3 is a 128x32 pixel LCD that has a viewing area of 36mm by 12mm, runs on 3.0V (up to 3.3V), and uses the SPI protocol. The graphics color is black and the background color is blue, and it includes a back-light powered by 3.0V. Each unit costs around \$12.

Newhaven Display's NHD-C12864LZ-FSW-FBW-3V3 is a 128x64 pixel LCD that has a viewing area of 70mm by 40mm, runs on 3.0V (up to 3.3V), and uses an 8-bit parallel interface, supporting both 6800 and 8080 modes. The graphics color is black and the background color is white, and it includes a back-light powered by 3.0V. Each unit costs around \$16.

Newhaven Display's NHD-C12864WC-FSW-FBW-3V3 is a 128x64 pixel LCD that has a viewing area of 58mm by 28.8mm, runs on 3.3V, and uses SPI or an 8-bit parallel interface, supporting both 6800 and 8080 modes. The graphics color is black and the background color is white, and it includes a back-light powered by 3.3V. Each unit costs around \$17. An option with screw tabs is available for the same price.

Refer to Table 3 for a chart comparing these modules.

The NHD-C12864WC-FSW-FBW-3V3 was selected. The medium-size screen with good pixel resolution will keep the form factor down while increasing pixel density. The typical operation of 3.3V and up to 3.6V will provide consistency with our other components. In addition, the screw tabs will be useful when integrating the final product.

4.6.2.2 Rotary Encoder with a Pushbutton

Bourns' PEC11-4215F-S24 is a rotary encoder with a pushbutton that has a 24-pulse encoder and is designed for audio applications. It includes a knob cap and each unit costs around \$5.

Bourns' PEC11R-4015F-S0018 is a rotary encoder with a pushbutton that has an 18-pulse encoder and is designed

Module	Cost	Viewing Area	Pixels	Color (Graphics, Background)	Backlight
NHD-C12832A1Z-FSB-FBW-3V3	\$12	36mm x 12mm	128x32	Black, Blue	3.0V
NHD-C12864LZ-FSW-FBW-3V3	\$16	70mm x 40mm	128x64	Black, White	3.3V
NHD-C12864WC-FSW-FBW-3V3	\$17	58mm x 28.8mm	128x64	Black, White	3.6V

Table 3: LCD Trades

for audio applications. Each unit costs around \$2.

Bourns' PEC12R-3220F-S0024 is a rotary encoder with a pushbutton that has a 24-pulse encoder and is designed for audio applications. Each unit costs around \$1.

The PEC12R-3220F-S0024 was selected due to its low cost.

4.7 Power Module

4.7.1 Design specification

The power module should use commercial battery, be rechargeable, and support alternate input through USB-C wall adapter which is common for phone chargers. It should supply power to the whole system with a lifetime of at least 4 hours. With the microcontroller active current $I_{uP} = 40mA$ and the rest of the system below this number, we have $I_{total} = 80mA$, and thus

$$Capacity_{battery} \geq I_{total} \cdot 4h = 320mAh \quad (1)$$

4.7.2 Trades and design choice

Lithium Polymer batteries are common for cellphones and are thus easily available. For microcontrollers, the common supply voltage is 3.3V. We looked into Lipo batterie of different capacities and found that a 1500mAh battery would provide sufficient slack room for the lifetime requirement, while having minimum marginal cost and reasonable dimensions. The Lipo battery uses a JST header, so we choose a B2B-PH-K-S(LF)(SN) JST male header, and a USB4125-GF-A USB-C jack as panel mount components on our board. We use the power module of BM83 to charge the battery and output 3.3V voltage to the whole board from the 3.7V battery supply, because this module is readily available to us together with its Bluetooth capabilities.

5 SYSTEM DESCRIPTION

5.1 Pre-Amplifier Module

The Pre-Amplifier Module schematic is shown in Fig. 2. As shown, audio input signals are accepted through a hybrid XLR / 1/4" jack. (The hot Tip and cold Ring wires are shorted to the hot 2 and cold 3 wires respectively to allow either XLR or 1/4" signals to be passed to the same input path.) The signal is then capacitively coupled to the MAX4061 audio amplifier, which converts it to single-ended (if necessary) and passes the output to

Signal	Direction	Description
CH<3:0>_SDB	INPUT GPIO	Active-low shutdown
SCL SDA	INPUT I2C	Digipot control bus

Table 4: Pre-Amplifier Interface

Signal	Direction	Description
EFFECT_SEL <3:0>	INPUT GPIO	Enable Analog Effect
SCL SDA	INPUT I2C	Digipot control bus

Table 5: Analog Effect Interface

the Audio Effect Module and ADC. A solder jumper is provided to optionally short the cable shielding to ground if this will provide better performance. The wires labeled PA_POT0W (Pre-Amplifier Potentiometer, Channel 0, Wiper) and PA_POT0A (Pre-Amplifier Potentiometer, Channel 0, Terminal A) connect to the MAX4451 digital potentiometer.

5.2 Analog Effect Module

The Analog Effect Module schematic is show in Fig. 3. Like the original Colorsound Overdriver pedal, our overdrive effect consists of three stages. The first stage drives the signal magnitude into the saturation region of the two BJTs, producing soft clipping and harmonic distortion (colloquially known as "Fuzz Face"). The second stage is a tone stack, which controls the relative amplitude of the Bass, Mid, and Treble bands. The third stage is purely an output buffer that sets the gain of the entire module. As with the pre-amplifier, the wires with labels in dashed gray boxes are potentiometer terminals.

5.3 Microcontroller

5.3.1 Interface

The microcontroller interfaces with all other modules and is already specified in other sections.

Our external ADC, which complements the microcontroller, interfaces with the microcontroller as specified in Table 6. The ADC is controlled through an I2C bus shared with the Pre-Amp module and Analog Effect module, and

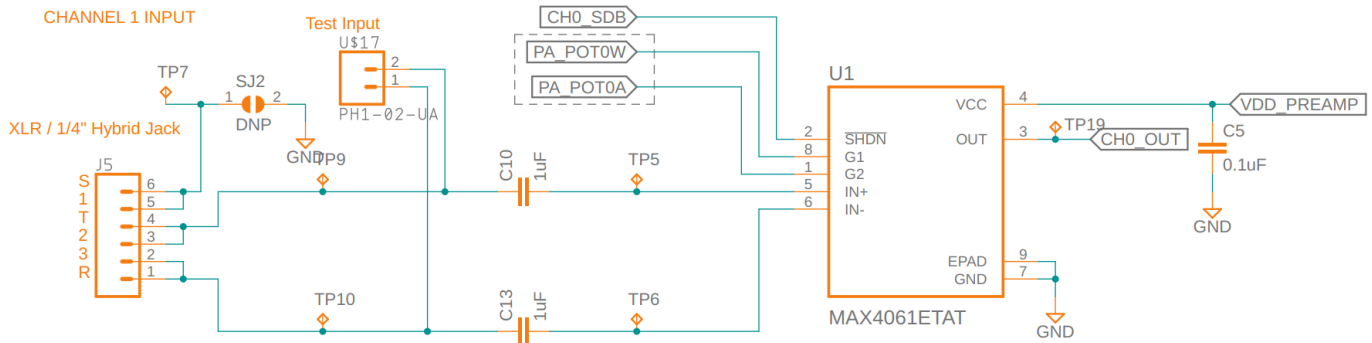


Figure 2: Pre-Amplifier Schematic

Signal	Direction	Description
MCLK	INPUT Clock	uP master clock
ADC_BCK ADC_LRCK ADC_DOUT	I/O SPI w/ TDM	commands and data
ADC_IRQ	OUTPUT Interrupt	interrupt output
SCL SDA	INPUT I2C	control (shared bus)
LED	OUTPUT LED	programmable LED

Table 6: ADC Interface

the data outputs through an SPI bus which is Time-division Multiplexed (TDM) across the 4 channels.

5.3.2 Control Software

The microcontroller processes the audio input stream and outputs them to the BM83 Bluetooth module. It also takes user inputs and controls the parameters of other modules. Fig. 6 shows the workflow of our microcontroller. In particular, the **Main Routine** manages the audio data flow, while the **Interrupt Routine** responds to user actions by outputting control signals to other modules, while having minimal effects on the latency of the **Main Routine**.

5.3.2.1 Data Flow

The microcontroller receives the ADC output through SPI bus with an additional Word Select (WS) line, which indicates the start of each time-division multiplexed frame containing 1 sample from each enabled input. The DSP algorithm will process the audio signal from the input buffer, and then store into output buffer. Then the processed signal is sent through I2S bus to the BM83 Bluetooth module.

Both the input and output interfaces use Direct Memory Access (DMA) in order to free the processor from heavy I/O and ensure low latency.

5.3.2.2 Control Signal

The control events are handled in interrupts and are triggered by user action. The user interacts with the rotary encoder or the foot switch, and the GPIO signal will inform the UI module to update the display parameters (which are drove to the LCD display in background by DMA). The UI module also parses the user input into actions, and the control module will base on these actions to output control signals to the Pre-Amp module (via GPIO and I2C), the Analog Effect module (via GPIO and I2C), and the Bluetooth module (via UART). The user inputs can also set the internal DSP parameters which takes effect immediately on the next processed block.

5.3.3 Digital Signal Processing

The digital effects will be implemented using a double-buffering scheme for both the input and output. This allows for block processing to reduce computational strain, still while inducing minimal latency. For 64 sample buffers, 2.9 ms of latency is induced by block processing, and for 256 sample buffers, 11.6 ms of latency is induced by block processing. The microcontroller has 192KB of SRAM, which will be used for storing wet and dry inputs, outputs, and computations. The microcontroller has 1MB of flash storage, which the digital effects will use to store filter coefficients and wavetables for low-frequency oscillators (LFOs).

5.3.3.1 Equalization

Equalization is used to shape the frequency response of an input. The 3-band equalization effect will be implemented using a low shelf filter with a cut-off frequency of 200Hz, a band pass filter centered at 1kHz, and a high shelf filter with a cut-off frequency of 5kHz. Shelf filters allow for a more even boosting or cutting across different frequencies, as opposed to low and high pass filters. A user will adjust the bass control to set the gain of the low shelf filter, the middle control to set the gain of the band pass filter, and the treble control to set the gain of the high shelf filter.

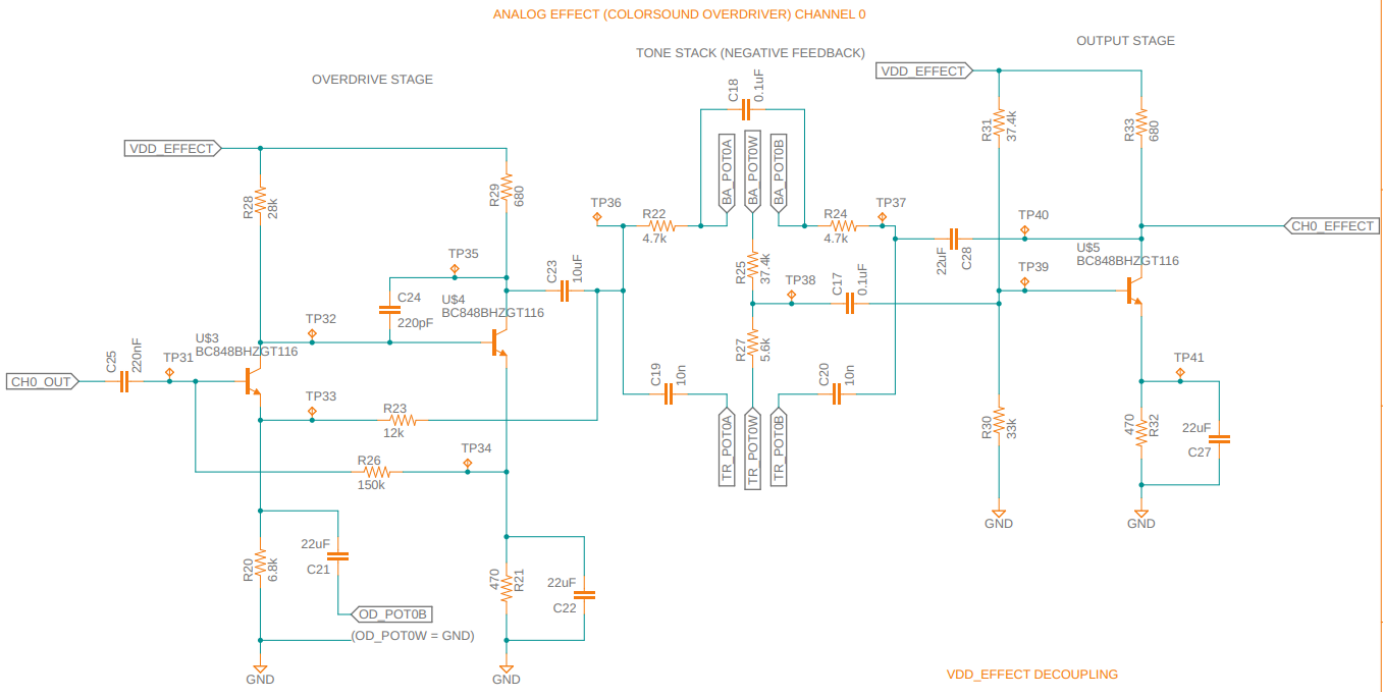


Figure 3: Analog Effect Schematic

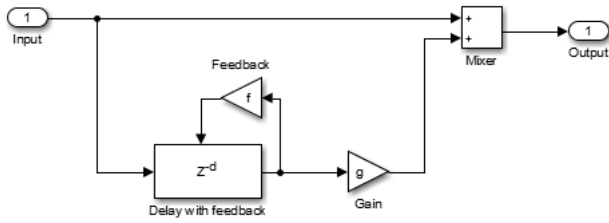


Figure 4: Delay Block Diagram

5.3.3.2 Delay

Delay is used to apply an artificial echo to a signal. The wet delay signal is implemented by delaying the sum of a feedback loop of the wet signal itself with a gain of less than 1 and the input signal. A gain of less than 1 is essential to provide a stable system and to produce a fading effect. The amount of delay is set by the user, up to 350 ms (S.R. 18). The output signal of the delay effect is determined by the wet/dry ratio set by the user, which tunes the gain of the wet and dry signals (S.R. 17). See Fig. 4 for a block diagram. [2]

5.3.3.3 Chorus

Chorus is used to add richness to a signal, simulating the sound of multiple instruments or vocals sounding simultaneously. The wet chorus signal is implemented by summing copies of the input signal, each delayed by a variable amount of delay set by separate LFOs. The modulation depth is set by the user and determines the range of amplitudes for the LFOs, and thus the potential amount of delays for each line in the wet signal (S.R. 19). The rate

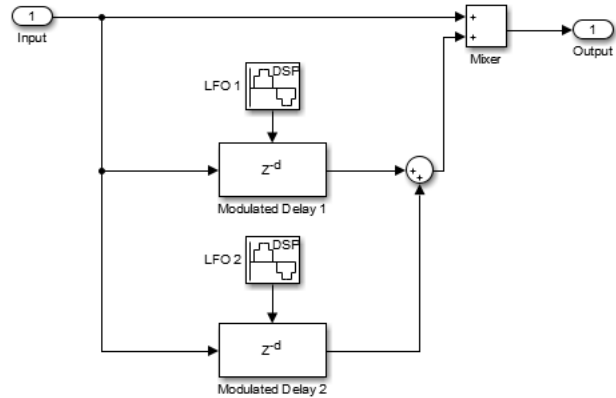


Figure 5: Chorus Block Diagram

also set by the user and determines the frequency of the LFOs, changing how quickly each delay is applied to the lines in the wet signal (S.R. 20). The output signal of the chorus effect is determined by the wet/dry ratio set by the user, which tunes the gain of the wet and dry signals (S.R. 21). See Fig. 5 for a block diagram. [2]

5.4 Bluetooth Module

5.4.1 Interface

Our Bluetooth module BM83 interfaces with the microcontroller as specified in Table 7. The Bluetooth receives audio input from the microcontroller via an I2S bus, and receives commands through UART.

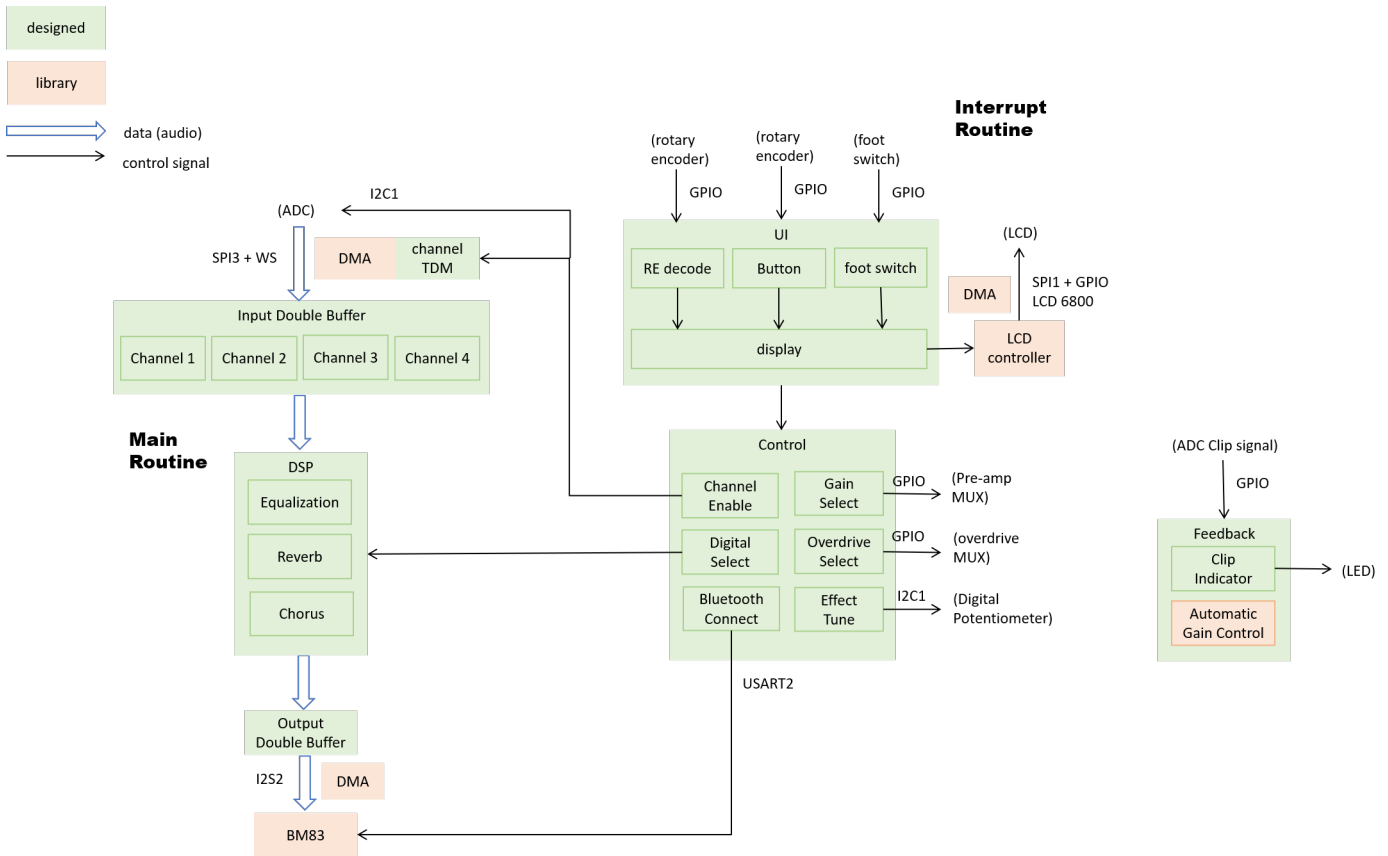


Figure 6: Software Block Diagram

Signal	Direction	Description
BT_RFS BT_SCLK BT_DR	INPUT I2S	Digital audio input
BT_RXD BT_TXD	IN/OUT UART	Bi-direction command
BT_MFB	INPUT GPIO	BM83 wakeup
BT_RSTB	INPUT GPIO	reset (active low)
BT_MCWAKE	OUTPUT GPIO	microcontroller wakeup

Table 7: BM83 Interface

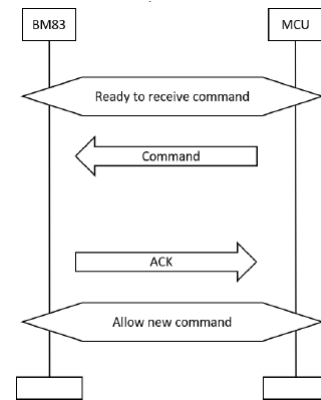


Figure 7: BM83 UART Handshake

5.4.2 Control Protocol

The BM83 has a handshake protocol for receiving commands through the UART interface. Fig. 7 shows an example message sequence for sending one command to the BM83 module [1].

Fig. 8 shows the example commands we can initiate to the BM83 module. Details of the command packet format can be found in the BM83 user guide [1]. As an example, we will be using the "Fast enter pairing mode" command to start pairing with Bluetooth speakers.

5.5 User Interface Module

5.5.1 Interface

The UI module interfaces with the microcontroller as specified in Table 8.

5.6 Power Module

The Power Module schematic is given in Fig. 9.

Signal	Direction	Description
LCD_SCK LCD_MOSI	IN/OUT SPI	Serial clock and data
LCD_CS1B	INPUT GPIO	Active low chip select
LCD_A0	INPUT GPIO	Register select
LCD_PS	INPUT	Parallel/serial select
LCD_RSTB	INPUT GPIO	Active low reset
RENC_A	OUTPUT GPIO	Encoder output channel A
RENC_C	OUTPUT	Encoder common output
RENC_B	OUTPUT GPIO	Encoder output channel B
BUTTON_T1	OUTPUT GPIO	Pushbutton output pin 1
BUTTON_T2	OUTPUT GPIO	Pushbutton output pin 2
FOOTSWITCH_T1	OUTPUT GPIO	Footswitch output pin 1
FOOTSWITCH_T2	OUTPUT GPIO	Footswitch output pin 2

Table 8: UI Interface

0x56	Reset some EEPROM setting to default setting
0x57	Force speaker gain toggle
0x58	Toggle button indication
0x5D	Fast enter pairing mode (from non-off mode)
0x5E	Switch power OFF
0x5F	Disable LED

Figure 8: BM83 UART Commands

5.6.1 Battery

The main power source for BARI is a 3.6V LiPo battery, which provides DC power to all other subsystems. The sense resistors R3R7 allow the power consumed by each subsystem to be independently measured. Additionally, the PGOOD LED U\$11 is illuminated if power to the system is switched on.

5.6.2 Charging

The 3.6V LiPo battery may be recharged through a 5V USB-C charging cable. The USB-C socket placed on the PCB is a poweronly socket which exposes only six pins. R1 and R2 are selected to comply with the USB-C protocol and D1 provides electrostatic protection for the system. A solder jumper is provided to optionally short the shield of the USB cable to the ground of the system. Note that the bat-

tery is not connected directly to the charging port: charging current and voltage is mediated by a battery charging circuit onboard the BM83.

6 PROJECT MANAGEMENT

6.1 Schedule

Our schedule is shown in Fig. 10. There have been no significant changes to the schedule since our proposal. The Rev 1 PCB was ordered the week of Mar 8 as planned, and we remain on track to finish the project with one week of slack time.

6.2 Team Member Responsibilities

Adam is primarily responsible for the hardware implementation of BARI. Over the past several weeks, he has downselected components, created a schematic and layout for the Rev 1 board, and placed the PCB order. He will also be responsible for designing the mechanical enclosure of the device as well as the schematics/layout for the Rev 2 PCB and the physical assembly and test of both hardware revisions.

Sam is primarily responsible for the implementation of the digital effects and user interface. Up until this point, he has created MATLAB prototypes for the effects we plan to implement, and he is now working to implement them on our embedded hardware. Later in the semester, he will work with Xingran on full signal path verification.

Xingran is primarily responsible for the software architecture on the microcontroller and BM83. She is currently working on high-level code architecture and interface bringup while we wait for the Rev 1 board. Once that arrives, she will shift to low-level implementation and test, finally doing full signal path verification with Sam at the end of the semester.

6.3 Budget

The overall budget for our project is given in Fig. 11. The two sections of the table specify which components are used for development and which are components that will become a part of our final product.

Notably, a large fraction of our budget is allocated to the fabrication of our Rev 1 and Rev 2 printed circuit boards. Details of how the budgeted fabrication cost was calculated (and other fabrication options we considered) are presented in Fig. 12. Finally, a bill of materials for the Rev 1 circuit board is presented in 13. The bill of materials for Rev 2 is expected to be very similar, with some modifications in the case that testing of Rev 1 reveals a design defect.

Even with extremely conservative estimates for the additional cost of the Rev 2 PCB and mechanical fabrication, we do not expect to use our full budget.

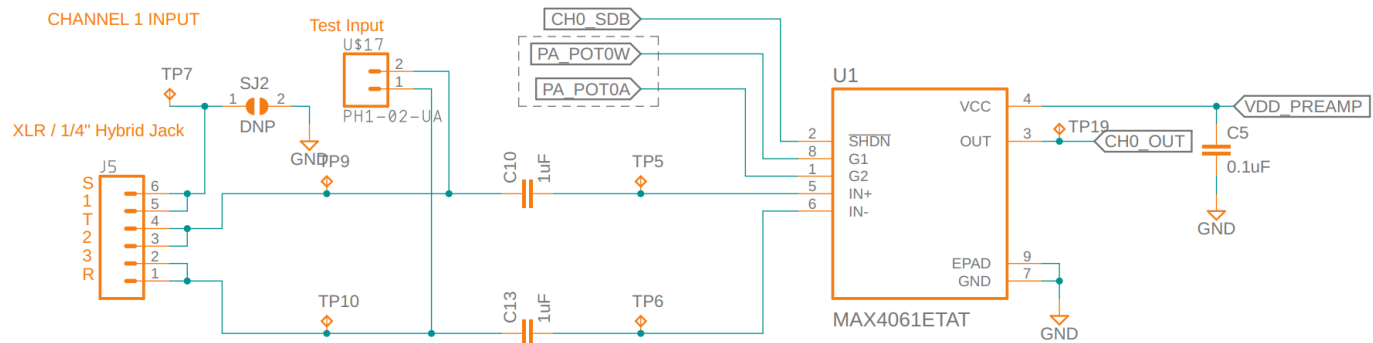


Figure 9: Power Module Schematic

6.4 Risk Management

The primary design and schedule risks that we face in this project are related to analog performance and system integration.

First, the analog performance of our design is difficult to verify before constructing our PCB, and exposes our final product to significant risk if it is unsatisfactory. We mitigate this risk by planning to fail quickly and recover if necessary. We have chosen to split our hardware design into two sequential revisions (Rev 1 and Rev 2) with the first scheduled to arrive before the end of March. We have prepared an exhaustive battery of functional tests and bringup procedures (see *BARI Test Procedure*) which we will apply to the Rev 1 board upon receiving it, exposing faults in time for modifications to be made for Rev 2. The Rev 1 board is also designed to be highly reworkable: it is only two layers, with most passive components in 0805 packages or larger and the ability to separate power rails for different modules, making it highly likely that at least some part of the Rev 1 board will be functional despite any hardware glitches.

The Rev 1 / Rev 2 schedule also helps to mitigate our second design risk (system integration) by providing a comparatively long time for integration and test with actual hardware. We have also secured development boards that feature the same STM32 processor used in our design with many of its peripherals, enabling basic software tests to be begun long before the Rev 1 boards arrive. From a software perspective, we are also pursuing a low-risk code architecture which abstracts hardware details into library functions, enabling most of the code base to be built before the hardware in question is received.

Prior to ordering our Rev 1 PCB, we also faced a resource risk in the form of unknown fabrication costs. However, at this point, we have already ordered components for the Rev 1 board, and barring a major redesign, these give us an excellent prediction for the cost of the components on the Rev 2 board. As mentioned in the previous section, we are able to finish our project within the allotted budget even with extremely conservative estimates for those costs which are yet to be incurred.

References

- [1] *BM83 Host MCU Firmware Development Guide*. A. Microchip Technology Inc. July 2019, pp. 31–32, 107–110.
- [2] The MathWorks Inc. *Delay-Based Audio Effects*. URL: <https://www.mathworks.com/help/audio/ug/delay-based-audio-effects.html>. (accessed: 03.17.2021).

Appendix A

Test Procedure	System Requirement
Battery Lifecycle Test	SR4 (Battery Lifetime)
System Power Consumption Test	(None, internal specification test)
Impedance Probe Test	SR8 (Input Impedance)
Pre-Amplifier Functional Test	SR7 (Input Signal Definition) SR9 (Pre-Amplifier Output) SR10 (Pre-Amplifier Gain Flatness) SR11 (Pre-Amplifier Distortion)
Analog Effect SPICE Verification Test	SR12 (Analog Overdrive Performance)
Digital Effect MATLAB Verification Test	SR15 (Minimum Digital Effects) SR16 (Equalization Quality) SR17 (Reverb Wet/Dry Ratio) SR18 (Reverb Time) SR19 (Chorus Modulation Depth) SR20 (Chorus Rate)
Processing Latency Test	SR21 (Digital Processing Latency)
User Interface Latency Test	SR22 (User Interface Response Latency) SR23 (User Interface Update Latency)
Bluetooth Range Test	SR14 (Bluetooth Transmission Range)
Ease-of-Use Test	SR24 (User Interface Interaction Time)
<i>All of the above tests:</i>	SR1 (Temperature)
<i>Ensured by Design:</i>	SR2 (System Form Factor) SR3 (System Cost) SR5 (System Voltage Supply) SR6 (Input Connector Definition) SR13 (Bluetooth Transmission Protocol) SR25 (User Interface Feedback Mechanism)

Table 9: Test Procedures vs. System Requirements

Appendix B

	1-Mar	8-Mar	15-Mar	22-Mar	29-Mar	5-Apr	12-Apr	19-Apr	26-Apr
Adam	Rev 1 Layout								
		Mechanical Design							F
				Rev 1 TEST					I
				Rev 2 Schem.				S	N
					Hardware Implementation			L	A
							HW Stress Test	A	L
Sam	MATLAB Effect Prototypes							C	
			Embedded DSP Implementation					K	P
					SW Unit Test				R
						Full Signal Path Test			E
						Interim Demo			S
Xingran	SW Arch.								E
		SW Low-Level Development							N
				SW Integration & Unit Test					T
						Full Signal Path Test			A
						Interim Demo			T
									I
		^ Order Rev 1	^ Design Report Due						O
		^ Design Presentation Due		^ Rev 1 Arrives	^ Order Rev 2		^ Rev 2 Arrives		N

Figure 10: Project Schedule

Appendix C

Item	Quantity	Unit Cost	Total Cost	Shipping	Vendor
Development Resources -----					
STM32F407G-DISC1	1	\$19.90	\$19.90	\$4.99	Digi-Key
Jumper wires	1	\$5.89	\$5.89	\$0.00	Amazon
JTAG Programmer	1	\$20.35	\$20.35		Digi-Key
Final Product -----					
LCD (NHD-C12864WC-FSW-FBW-3V3-M)	2	\$16.85	\$33.70		Digi-Key
Rotary Encoder w/ button (PEC12R-3220F-S0024)	2	\$1.17	\$2.34		Digi-Key
3.7V Lipo	2	\$9.19	\$18.38	\$0.00	Amazon
Footswitch (2 pack)	1	\$8.63	\$8.63	\$0.00	Amazon
XLR/TRS Connectors	8	\$3.25	\$26.00	\$6.99	Amazon
TRS output	1	\$1.10	\$1.10		Digi-Key
Power Switch	2	\$1.10	\$1.10		Digi-Key
Rev1 Fabrication (See Page 2)	1	\$103.52	\$103.52		
Rev2 Fabrication (ESTIMATE)			\$180.00		
Budget for Mechanical Assembly (ESTIMATE)	1	\$100.00	\$100.00		
		Total	\$520.91	\$11.98	
		Budget	\$600.00		
		Surplus/Deficit	\$ 67.11		

Figure 11: Project Budget

	<i>PCBWAY</i>	<i>JLCPCB (1.5 boards)</i>	<i>JLCPCB (2 boards)</i>	<i>Assemble 1 bare board</i>	<i>Assemble 2 bare boards</i>
PCB Fabrication	\$5.00	\$2.00	\$2.00	\$2.00	\$2.00
Lead Time	4-5 days	2-3 days	2-3 days	2-3 days	2-3 days
SMT Assembly	\$88.00	\$10.37	\$10.37	\$0	\$0
Lead Time	25-30 days	72 hours	72 hours		
Fab-soldered Components	\$104.00	\$21.19	\$21.19		
Adam-soldered Components	\$0	\$27.08	\$54.16	\$50.41	\$100.82
	(0 components)	(30 components)	2 x (30 components)	(~150 components)	2 x (~150 components)
Shipping (PCB only)	\$0	\$15.80	\$15.80	\$15.80	\$15.80
	DHL (3-7 days)	DHL Express (2-4 business days)	DHL Express (2-4 business days)	DHL Express (2-4 business days)	DHL Express (2-4 business days)
TOTAL	\$197.00	\$76.44	\$103.52	\$68.21	\$118.62

Figure 12: Rev 1 PCB Cost Breakdown

MFG Part Number	Designator	Quantity	Footprint	Manufacturer	Description	Type(SMD/THT)
150060RS75000	U\$11, U\$12	4	0603	Würth Elektronik	LED RED CLEAR 0603 SMD	SMD
74LV4053D,118	IC1	1	16-SOIC	Nexperia USA Inc	Triple 2:1 Mux	SMD
B2B-PH-K-S(LF)(SN)	U\$2, U\$21	2	2mm THT	JST Sales America	CONN HEADER VERT 2POS 2MM	THT
BC848BHZGT116	U\$3, U\$4, U	6	SOT-23-3	Rohm Semicondu	NPN GENERAL PURPOSE TRANSISTOR	SMD
BM833M1	U\$1	1	50-SMD	Microchip Techno	Bluetooth Module	SMD
C0805C103J5RAC7800	C19, C20, C3	6	0805	KEMET	CAP CER 10000PF 50V X7R 0805	SMD
CL05B104KO5NFNC	C2, C5, C6, C	21	0402	Samsung Electro	CAP CER 0.1UF 16V X7R 0402	SMD
CL21A106KOQNNNG	C1, C14, C15	11	0805	Samsung Electro	CAP CER 10UF 16V X5R 0805	SMD
CL21A226MQQNNNE	C11, C21, C2	10	0805	Samsung Electro	CAP CER 22UF 6.3V X5R 0805	SMD
CL21B105KOFNNNG	C3, C4, C8, C	17	0805	Samsung Electro	CAP CER 1UF 16V X7R 0805	SMD
CL21B224KBFNNNE	C25, C37	2	0805	Samsung Electro	CAP CER 0.22UF 50V X7R 0805	SMD
CL21B225KPFNNNE	C74, C75	2	0805	Samsung Electro	CAP CER 2.2UF 10V X7R 0805	SMD
CL21C221JBANNNC	C24, C36	2	0805	Samsung Electro	CAP CER 220PF 50V COG/NPO 0805	SMD
RMCF1206JT4R70	R8, R56, R57	4	1206	Stackpole Electro	4.7 Ohms ±5% 0.25W, 1/4W Chip Resistor 1206	SMD
CRCW080537K4FKEA	R25, R31, R3	4	0805	Vishay Dale	RES SMD 37.4K OHM 1% 1/8W 0805	SMD
CRG0805F150K	R26, R40	2	0805	TE Connectivity Pa	RES SMD 150K OHM 1% 1/8W 0805	SMD
CRG0805F6K8	R20, R34	2	0805	TE Connectivity Pa	RES SMD 6.8K OHM 1% 1/8W 0805	SMD
CRGCQ0805F12K	R23, R36, R5	8	0805	TE Connectivity Pa	CRGCQ 0805 12K 1%	SMD
CRGCQ0805F33K	R30, R44	2	0805	TE Connectivity Pa	CRGCQ 0805 33K 1%	SMD
CRGCQ0805F470R	R21, R32, R3	4	0805	TE Connectivity Pa	CRGCQ 0805 470R 1%	SMD
CRGCQ0805F5K6	R27, R41	2	0805	TE Connectivity Pa	CRGCQ 0805 5K6 1%	SMD
CRGCQ0805F680R	R29, R33, R4	4	0805	TE Connectivity Pa	CRGCQ 0805 680R 1%	SMD
ERA-6AED472V	R22, R24, R3	4	0805	Panasonic Electro	RES 4.7 KOHMS 0.5% 1/8W 0805	SMD
ESD233B1W0201E6327X	D1	1	0201	Infineon Technolo	TVS Diode	SMD
MAX4061ETA+T	U1, U2	2	8-TDFN-EF	Maxim Integrated	IC AMP CLASS AB MONO 8TDFN	SMD
MCP4451-104E/ST	U4, U8	2	20-TSSOP	Microchip Techno	IC DGT POT 100KOHM 257TP 20TSSOP	SMD
PCM1864DBTR	U3	1	30-TSSOP	Texas Instrument	IC ADC/AUDIO 24BIT 192K 30TSSOP	SMD
PH1-02-UA	U\$10, U\$14	7	2.54mm T	Adam Tech	CONN HEADER VERT 2POS 2.54MM	THT
PH1-06-UA	J2, J3, J4, J5,	5	2.54mm T	Adam Tech	CONN HEADER VERT 6POS 2.54MM	THT
RK73H2ATTD5101F	R1, R2	2	0805	KOA Speer Electr	RES 5.1K OHM 1% 1/4W 0805	SMD
RMCF0805FT28K0	R28, R42	2	0805	Stackpole Electro	RES 28K OHM 1% 1/8W 0805	SMD
RMCF1206FT1R00	R3, R4, R5, R	5	1206	Stackpole Electro	RES 1 OHM 1% 1/4W 1206	SMD
RNCP0805FTD2K49	R61, R62	2	0805	Stackpole Electro	RES 2.49K OHM 1% 1/4W 0805	SMD
RT0805FRE0714ORL	R48, R49, R5	4	0805	Yageo	RES SMD 140 OHM 1% 1/8W 0805	SMD
SFV30R-3STBE1HLF	U\$9	1	30pos 0.5	Amphenol ICC (FC	CONN FPC BOTTOM 30POS 0.50MM R/A	SMD
STM32F407VGT6	U7	1	100-LQFP	STMicroelectroni	IC MCU 32BIT 1MB FLASH 100LQFP	SMD
USB4125-GF-A	J1	1	USB-C Boæ	GCT	USB C REC, GF, RA, 6P, SMT, TH S	SMD & THT

Figure 13: Rev 1 PCB Bill of Materials