Misc. Notes:

- I2C SCL Clock Frequency of 100KHz and 400KHz supported.
- 400KHz works and has been tested (3/5/21). Oddly, the default for the HDMI_TX CD example is 20KHz, which has also been tested and works (2/27/21).

How much to divide our reference clock by to achieve 400KHz?
f_fpga = 50 MHz
f_i2c = 400kHz
f_fpga/f_i2c = 125
Use a counter to divide our SCL clock line frequency by 125 to get a 400KHz clock.

0x15	R/W	[7:4]	0000****	I2S Sampling Frequency (CS bits 27-24)	Sampling frequency for I2S audio. This information is used by both the audio Rx and the pixel repetition. 0000 = 44.1 kHz 0001 = Do not use 0010 = 48.0 kHz 0011 = 32.0 kHz 0100 = Do not use 0101 = Do not use 0110 = Do not use 0111 = Do not use 1000 = 88.2 kHz 1001 = HBR Audio 1010 = 96.0 kHz 1011 = Do not use 1100 = 176.4 kHz 1101 = Do not use 1110 = 192.0 kHz 1111 = Do not use	4.4.3
		[3:0]	****0000	Input ID	Input Video Format See ►Table 16 to ►Table 21 0000 = 24 bit RGB 4:4:4 or YCbCr 4:4:4 (separate syncs) 0001 = 16, 20, 24 bit YCbCr 4:2:2 (separate syncs) 0010 = 16, 20, 24 bit YCbCr 4:2:2 (embedded syncs) 0011 = 8, 10, 12 bit YCbCr 4:2:2 (2x pixel clock, separate syncs) 0100 = 8, 10, 12 bit YCbCr 4:2:2 (2x pixel clock, embedded syncs) 0101 = 12, 15, 16 bit RGB 4:4:4 or YCbCr (DDR with separate syncs) (0xD0[3:2] must be set to 2'b11) 0110 = 8,10,12 bit YCbCr 4:2:2 (DDR with separate syncs) (0xD0[3:2] must be set to 2'b11) 0111 = 8, 10, 12 bit YCbCr 4:2:2 (DDR separate syncs) (0xD0[3:2] must be set to 2'b11) 1000 = 8, 10, 12 bit YCbCr 4:2:2 (DDR embedded syncs)	4.3.1

Above: Configuration details from [0, pg. 135].

- Video and audio format is configured in one 8-bit register.

How to write to I2C Registers:

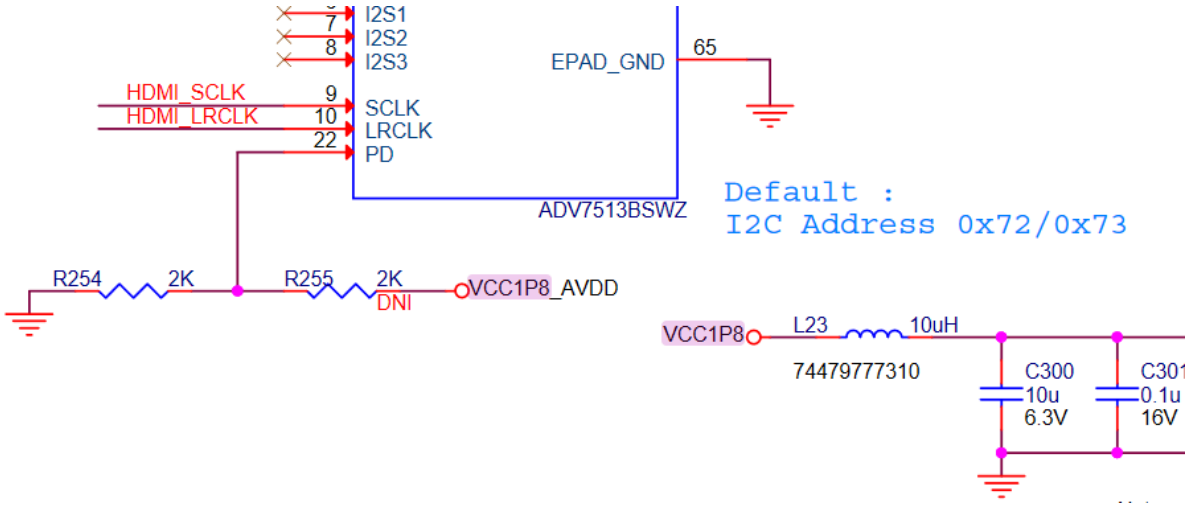
- The address to write to for accessing the main register map depends on whether there is a pull down resistor to GND or pull up resistor to AVDD. If the PD/AD pin pull down to

GND when power is applied to the ADV7513, then write to 0x72. If PD/AD is pulled high when power is applied to the ADV7513, then write to 0x7A instead [0, pg. 15][2, pg. 30].

- The example code in HDMI_TX example from the online CD always writes to 0x72. I think it is safe to assume a fixed pull down resistor and that the address to write to is always 0x72 for our purposes.

PD/AD State at Startup:

- Important to know since it determines the default I2C base address for the ADV7513.



Above: Schematic diagram (sheet 21) of de10-nano board. From the downloadable CD.

- Can confirm from the schematic above that the default I2C address to use is **0x72**. The schematic includes a (2K) pull-down resistor to GND as recommended by [2, pg. 30]. The pull up resistor in the diagram has a DO NOT INSTALL (DNI), and so PD should always be low at power up.
- This means that we cannot change the I2C main register map address. It doesn't really matter much for us anyways.

Mandatory power-up sequence:

Source can be found in quick start guide [0, pg. 14]. Anywhere you see X below is a "don't-care", but the safest option (and the one the demo uses) is to set any X bit to 0.

Register to Modify	**Value to Use**	**Purpose**
0x41	0bX001_0000 **(use 0x10)**	Power on
0x98	0x03	Must be set to fixed value
8'h9A	0b1110_000X **(use 0xE0)**	Must be set to fixed value
8'h9C	0x30	Must be set to fixed value
8'h9D	0x61	Must be set to fixed value

8'hA2	0xA4	Must be set to fixed value
8'hA3	0xA4	Must be set to fixed value
8'hE0	0xD0	Must be set to fixed value
8'hF9	0x00	Must be set to fixed value

Audio Configuration Notes:

- Since we are targeting 32KHz audio (not the default for ADV7513), we will need to stray from the demo's implementation.
- There are a bunch of registers to set now. I will be detailing them here.

- 0x01, 0x02, 0x03: These registers form a 20-bit number which sets N for Audio Clock Regeneration [0, pg. 78].
    - Register 0x01 is allocated bits [19:16].
    - Register 0x02 is allocated bits [15:8].
    - Register 0x03 is allocated bits [7:0].
    - See [0, pg. 138] for more details on how bits are assigned to each register.
    - We must use the highlighted values in the table since they are closest to our 25MHz pixel clock.

Table 58 Recommended N and Expected CTS Values for 32KHz Audio

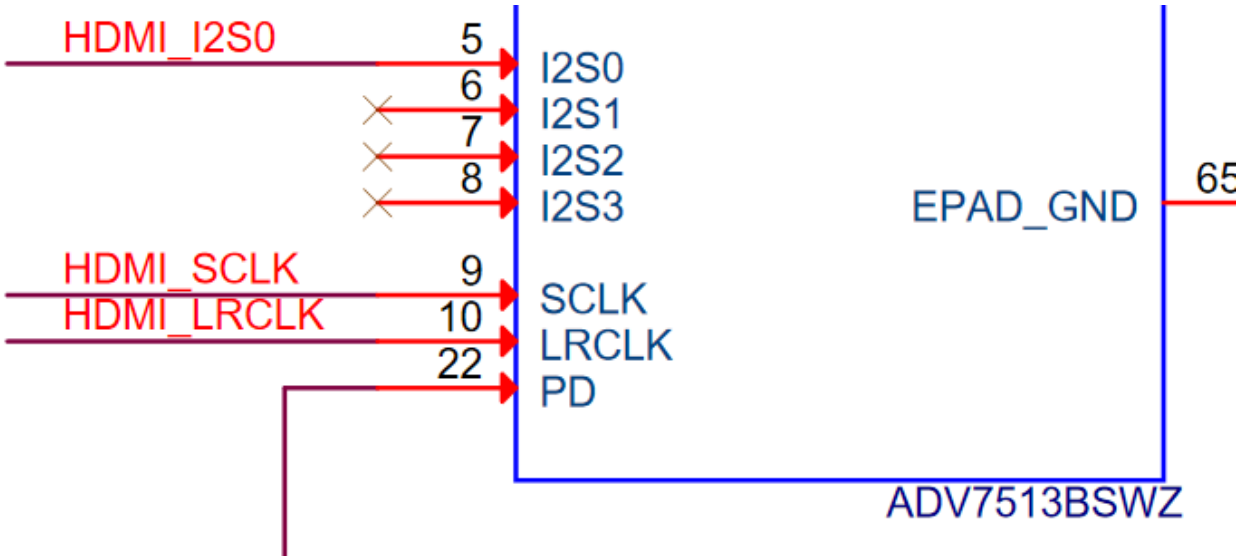
	32KHz	
Pixel Clock (MHz)	**N**	**CTS**
25.2 / 1.001	4576	28125
25.2	4096	25200
27	4096	27000
27 * 1.001	4096	27027
54	4096	54000
54 * 1.001	4096	54054
74.25 / 1.001	11648	210937 – 210938
74.25	4096	74250
148.5 / 1.001	11648	421875
148.5	4096	148500
Other	4096	Measured

Above: Table of recommended N and CTS values for 32KHz Audio [0, pg. 79]

- 0x07, 0x08, 0x09: These registers form another 20-bit number which sets CTS for Audio Clock Regeneration [0, pg 78]. Again, use the highlighted values in the table above.
    - Register 0x07 is allocated bits [19:16].
    - Register 0x08 is allocated bits [15:8].
    - Register 0x09 is allocated bits [7:0].
    - See [0, pg. 138] for more details on how bits are assigned to each register.

- 0x0B: Leave as default.
    - No SPDIF receiver.
    - Rising edge latched I2S SCLK polarity. This is for standard I2S [0, pg. 69 footnote].
    - MCLK is internally generated. MCLK is not required for standard I2S. See [0, table 53 pg. 69].

- 0x0C: Set to 0b1000_0100 = 0x84
    - Uses I2S sampling frequency set in 0x15.
    - Channel Status override register setting doesn't matter since we are not using I2S mode 4 (see table of I2S modes [0, pg. 69, table 53]).
    - The default settings enable all 4 I2S channels (I2S3, I2S2, I2S1, I2S0). We only need I2S0 though, since the others are disconnected! See diagram below:



Above: Diagram from online CD showing all I2S lines other than I2S0 are disconnected.
    - The default setting is to use Standard I2S Mode.

- 0x15: Bits [7:4] set the I2S Sampling Frequency. This register also controls the video format too, so be sure to assign them both at the same time.
    - Must set to 8'b0011_0000 (4 MSBs specify 32KHz audio, the 4 LSBs specify 24-bit RGB video)
- TODO 0x14
- TODO 0x40 AV Mute support? Demo enables this
- 0x73 Audio channel count for Audio InfoFrame. Set to 0b0000_0001 = 0x01 for 2 channels (ANSWER 3/6/21: Only HDMI_I2S0 is connected. So only 2 channels are being used).
- 0x76: NO NEED TO SET. More audio infoframe stuff. Specifically, it tells the audio receiver how many speakers to set up and what positions (front left, front right, right center, rear left, etc.) to use. Set to 0x00 **(DEFAULT)** to enable Front-left and Front-Right only for our two channel setup (see [0, pg. 87, table 64] for source).

Summary table:

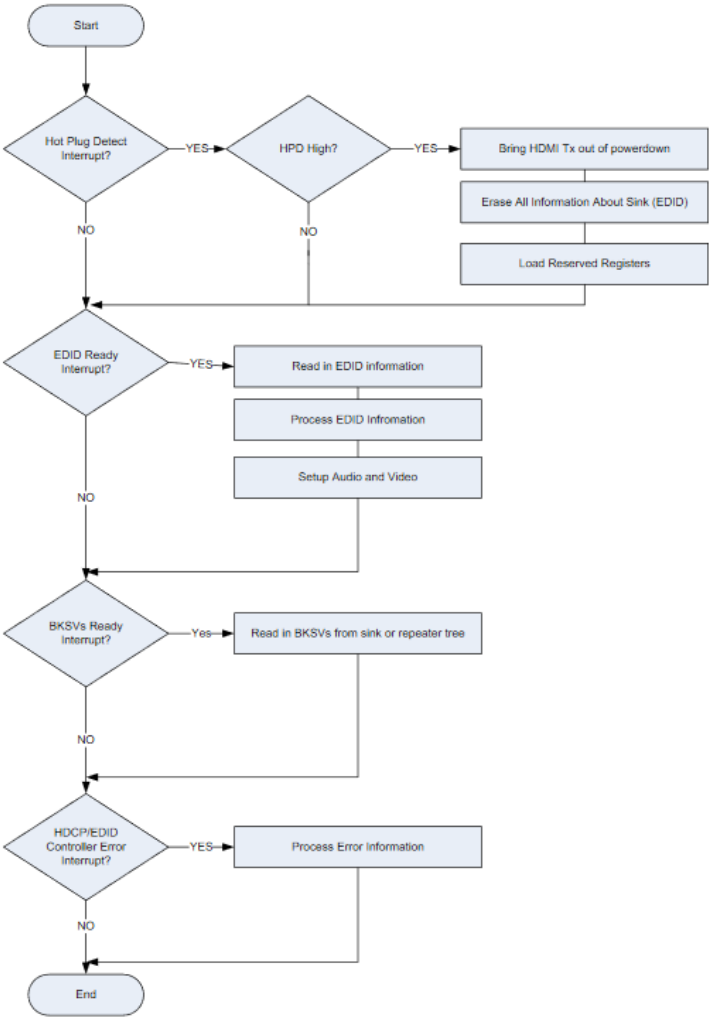
Register to Modify	**Value to Use**	**Purpose**
0x01	0x00	Setting N [19:16]
0x02	0x11	Setting N [15:8]
0x03	0xE0	Setting N [7:0]
0x07	0x02	Setting CTS [19:16]
0x08	0x81	Setting CTS [15:8]
0x09	0x25	Setting CTS [7:0]
0x0C	0x84	Disable all I2S channels other than I2S0.
0x15	0x30	32KHz I2S Sampling Frequency **(THIS OVERLAPS WITH THE VIDEO SETTING. Only need to set once)**
0x73	0x01	Tell audio InfoFrame we have 2 channels (I2S0)

Video Configuration Notes:

- 0x15: Bits [3:0] specify 24-bit RGB with Hsync and Vsync video input format if left as 0s. This overlaps with the audio sampling frequency setting.
- 0x16: Output video format. No need to set [3:2] for 4:4:4 RGB input style [0, pg. 27].
- 0x17: No need to set. Defaults to 4:3 aspect ratio, which is what we want for 640:480.
- 0x18. No need to set. Color Space convertion is disabled by default. Default settings okay
- 0xAF. Set bit [1] to 1 to enable HDMI mode. Other bits should be left as defaults (0'b0001_0110). Leave bit [7] at 0 since we do not care about enabling/supporting HDCP.
- 0x97. Leave bit [6] alone. We do not care about HDCP support.
- 0x55. Set to 0x10 to confirm RGB format for AVI Infoframe (I believe this is how the monitor identifies certain things about video/color format). Read about InfoFrame here: https://thedigitallifestyle.com/w/index.php/2010/03/26/making-sense-out-of-hdmi-1-4-performance-and-the-ceas-861-infoframes-installment-027/
- 0x56. Set to 0x18 to tell AVI InfoFrame about Picture Aspect Ratio and Active Format Aspect Ratio (not sure what the difference is). Specifically, we tell it that our picture has a 4:3 aspect ratio and the active format is the same as the picture.

- 0x96: Enable the following interrupts by setting to 0xF6:
    - HPD Interrupt (good to reset the configuration when hot-plug detection occurs).
    - Monitor sense interrupt.
    - Vsync Interrupt
    - Audio FIFO Full interrupt
    - EDID Ready Interrupt
    - HDCP Interrupt
    - TODO We really don't need EDID or HDCP support, so we don't really care to use this.
    - EDID is helpful because it allows your HDMI device to know what resolutions/display-tech the monitor supports, and so it can adapt on the fly. It is pretty complicated for this project though.

Figure 33 **Interrupt Handling Example**



- See the above diagram for the "HDMI Handshake" as it is called. Supporting this would be a stretch goal and isn't strictly necessary for this project.
- 0xBA: Set to 0x60 to set input video clock delay to 0. Setting to 0x70 works as well. It doesn't really matter since this is for the HDCP part.

Summary Table

Register to Modify	**Value to Use**	**Purpose**
0x15	0x30	24-bit RGB with Hsync and Vsync video input format **(THIS OVERLAPS WITH THE AUDIO SETTING. Only need to set once)**
0x16	0b0011_XX00 **(Use 0x30)**	Sets 4:4:4 RGB input style
0xAF	0x16	Enables HDMI mode
0x55	0x10	Setup AVI InfoFrame (maybe optional)
0x56	0x18	Tell AVI InfoFrame about Aspect ratios.
0xBA	0x60 or 0x70	Set video input clock delay to 0

Resources

[0] ADV7513 HDMI TX Controller Programming Guide
https://www.analog.com/media/en/technical-documentation/user-guides/ADV7513_Programming_Guide.pdf

[1] For refresher on I2C, see this guide.
https://www.circuitbasics.com/basics-of-the-i2c-communication-protocol/

[2] ADV7513 HDMI TX Controller Hardware Guide
https://www.analog.com/media/en/technical-documentation/user-guides/ADV7513_Hardware_User_Guide.pdf

[3] I2C FSM and other helpful descriptions
https://www.ijsr.net/archive/v4i1/SUB15631.pdf