Communications

Our address range is 0xC0000000-0xFC000000.
This corresponds to hps2fpgaslaves interface [0, section 31]. Uses the HPS2FPGA AXI Bridge.
Footnote: We're going to need to ask Linux for 1:1 mapped addresses

APU:

Base address: 0xF0000000
Offsets:

- 0x00 (WO): Address of the next buffer to be played in memory. If no buffer is known, no sound will be played. An interrupt will be sent when there is no buffer ready for after the currently playing buffer finishes.

PPU:

Base address: 0xF4000000
Offsets:

- 0x00 (WO): Control (enable/disable for each layer), high 29 bits reserved.
- 0x04 (WO): Address of palette memory in DRAM
- 0x08 (WO): Universal Background Color. Bits 31-24 are reserved.
- 0x0C (WO): Address of tile table in DRAM
- 0x10 (WO): Address of OAM in DRAM
- 0x14 (WO): Address of FG layer nametable in DRAM
- 0x18 (WO): FG scroll, Bits 31-25 and 15-9 are reserved, laid out in x, y.
- 0x1C (WO): Address of BG layer nametable in DRAM
- 0x20 (WO): BG scroll, Bits 31-25 and 15-9 are reserved, laid out in x, y.

Palette:

(FG/BG) 2 sets of 16 24-bit colors, with the 0th color being ignored (transparency).
(Sprites) 1 set of 32 24-bit colors, with the 0th color being ignored (transparency).

Scrolling:

We need to specify the base address of each tile layer, and an 8 pixel offset from that base address in each direction (forward/downward). Additionally, we'll need to inform the PPU what value it should add to the base address to advance one line down (to enable variable window sizing).

Sizing of FG/BG (nametables):
10 tile bits + 4 palette bits + 2 mirroring bits
= 16 bits

Sizing of sprite data (OAM):
10 tile bits + 5 palette bits + 9 bit x + 8 bit y = 32 bits

Sizing of additional sprite data (OAM):
2 mirroring bits + 2 tile width bits + 2 tile height bits + 2 bit fg/bg priority = 8 bits.

Note that the 4th state of priority “behind background & in front of foreground” is invalid. Defaults to “in front of both foreground and background”.
This data is appended to the end of OAM after the regular 32-bit sprite data. Addressed separately.

Other possible PPU MMIO:

- Enable/disable for individual layers
- Universal background color
- Universal sprite size option
- Individual palettes for each layer

INPUT:

Base address: 0xF8000000
Offsets:

- 0x0 (RO): Read current 16-bit controller state. High 16-bits are reserved (set to 0)

Resources

[0] Cyclone V HPS Manual (USE THE ONLINE VERSION, NOT THE ONE INCLUDED WITH THE ONLINE CD).
https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/hb/cyclone-v/cv_5v4.pdf