

Game Boy Emulation on FPGA

Game Boy - Team C0:

Tess (Therese) Chan

Pratyusha Duvvuri

Adolfo Victoria

Application Area

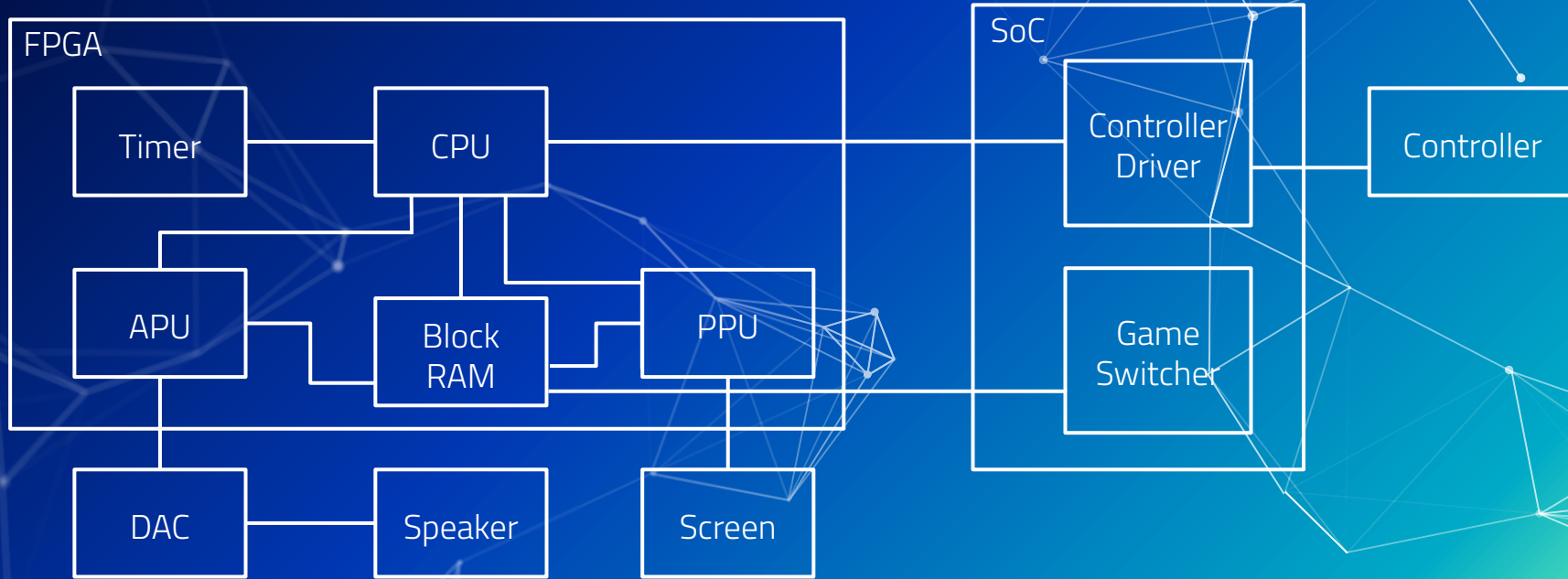
- Creating a cycle accurate Game Boy emulator on an FPGA
- Recreating classic systems on modern hardware to learn how older systems were implemented
- Areas: Hardware, Software



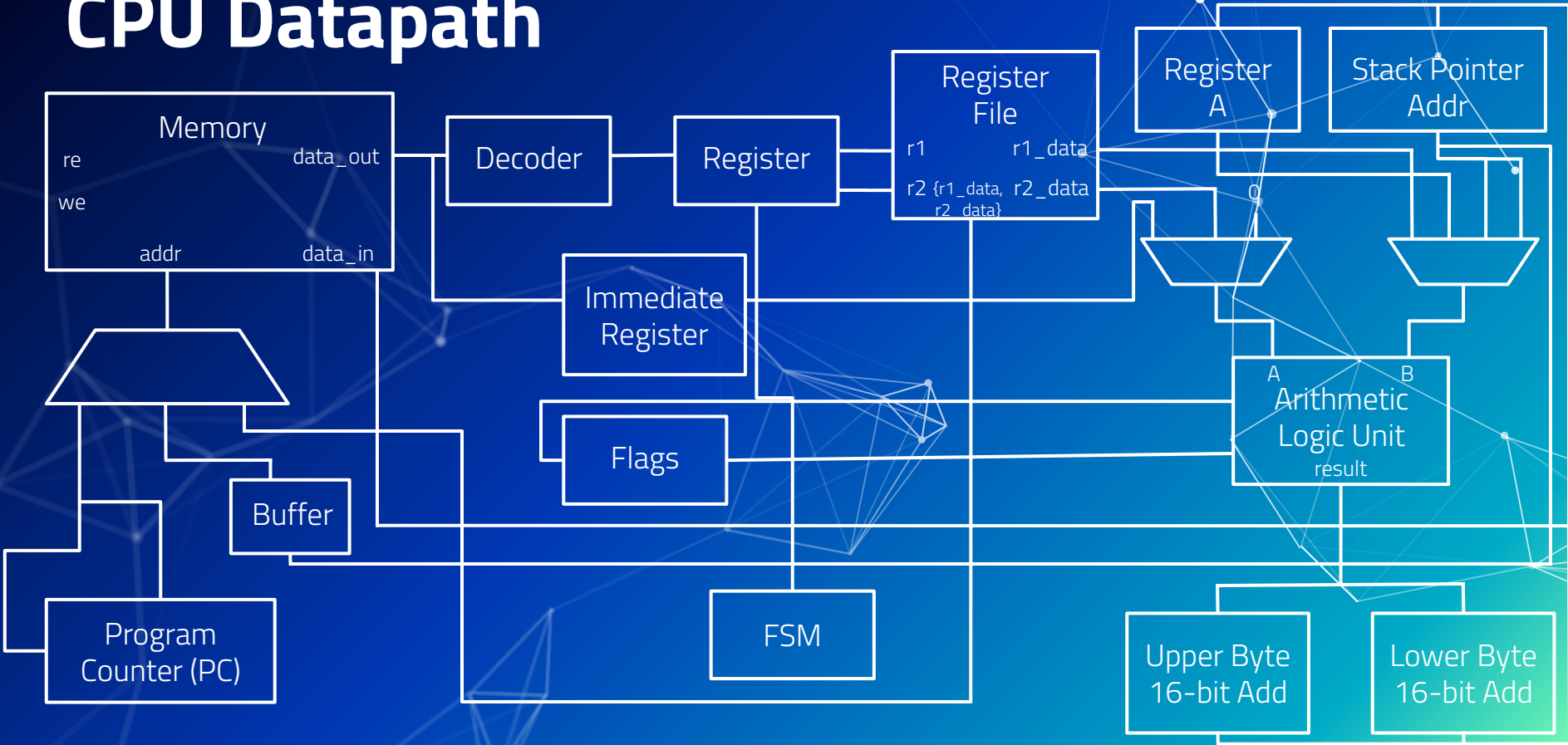
Solution Approach

- Use DE10-Standard development board with on board FPGA and System On Chip (SoC)
 - SoC will handle: controller inputs and game switching
 - FPGA will handle: CPU, APU, PPU, and Timer
- Create Game Boy emulator that will perform as well or better than the original console

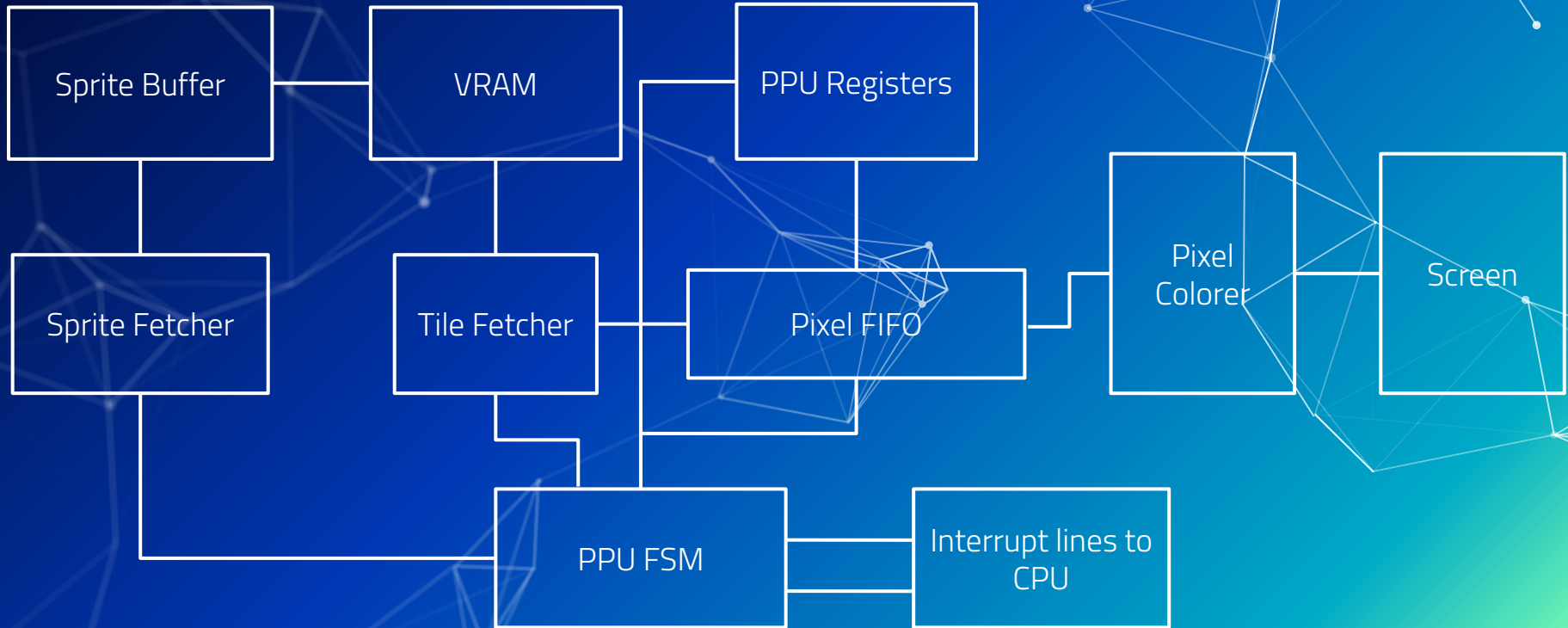
Overall System Block Diagram



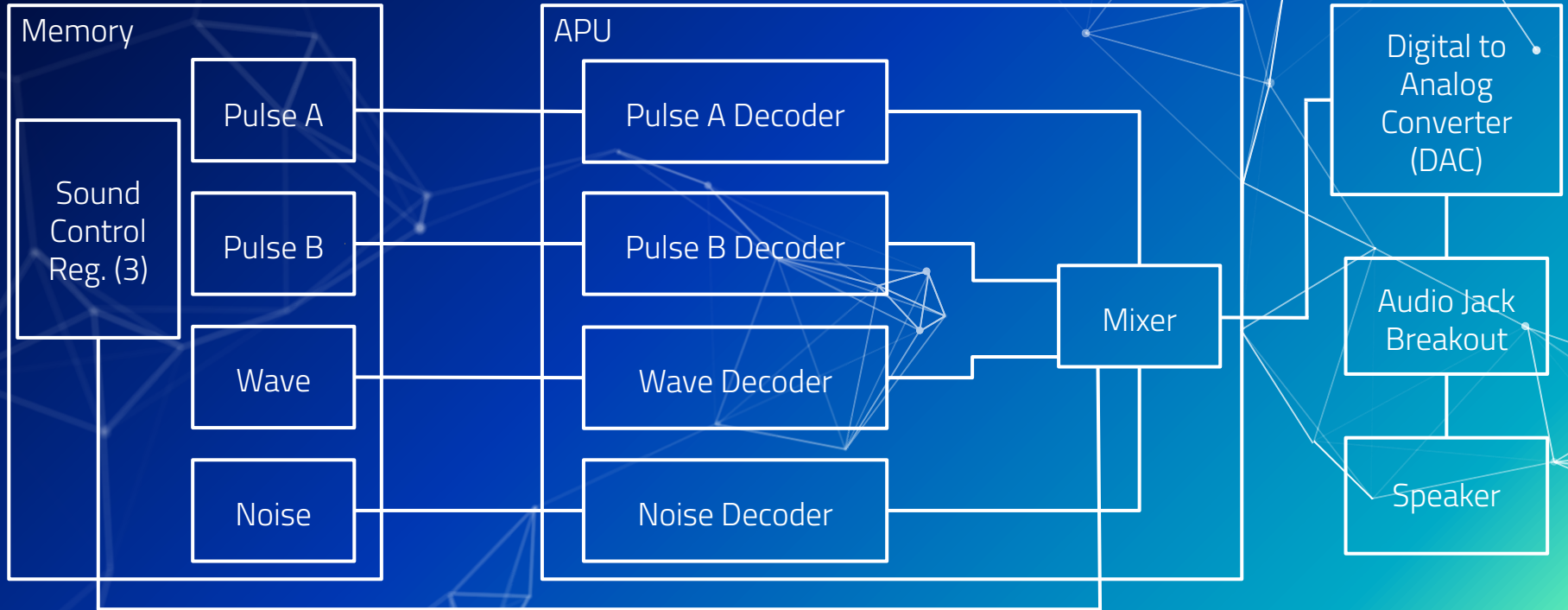
CPU Datapath



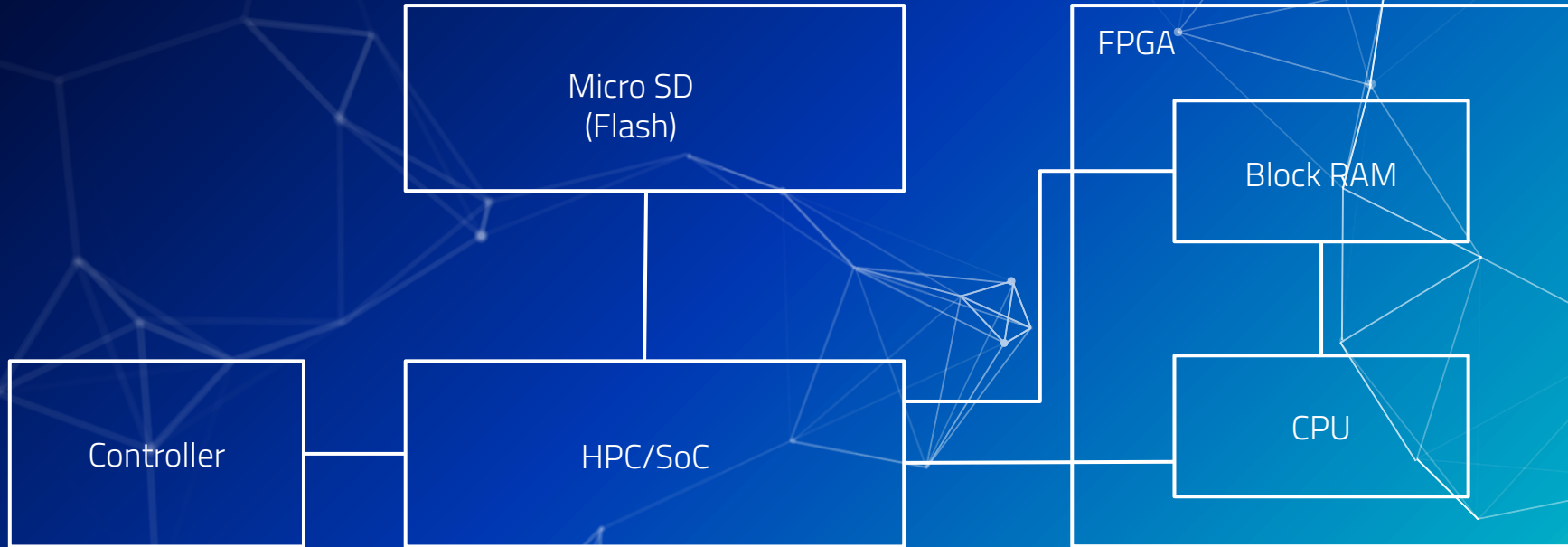
Block Diagram - Graphics



Block Diagram - Sound



Block Diagram - SoC



Anticipated Parts List

Part	Anticipated Cost	Status
AD669 DACPORT	\$40	Ordered
Audio Jack Breakout Board	\$15 (for 3)	Ordered
DE10-Standard Development Board	\$355*	Received
NES Controllers	\$12	Ordered
Micro SD Card	~\$20	To be selected
Speaker	TBD	To be selected

*Is not subtracted from our team budget

Metrics and Validation

- We will compare our performance to existing designs
 - Signal trace a tested and verified emulator and compare the log to our emulator performing the same tasks
- We will use online test suites for unit testing different components
 - The tests are pass/fail

Risk Factors

■ Integration

- Interface between individual components may not be synced
- Timing mismatch
- Solution: Try to design interfaces to integrate each part as soon as we finish an area of it that talks with other parts of the system

■ Overlooked unique cases

- Solution: Research in advanced known unique cases

■ Poor Documentation

- What we're basing our work on is based off of experiments and not ground truth

Schedule

We will continue using the Gantt chart proposed in the project proposal.

