hardware-README.md

Notes on Hardware

- To use Vivado, add the following line to your `.bashrc` or equivalent:

```
source ~/Private/SeamCarvingInTime/hardware/setup_vivado
```

- Pin assignment file (.xdc, Xilinx design constraints) can be found at xilinx.com/zc706.
- After running synthesis and implementation, Vivado will give you a critical warning for every pin in the .xdc file that your design doesn't use (`'set_property' expects at least one object.`), which is because `[get_ports PIN_NAME]` doesn't return a valid object. You can ignore this warning, or comment out unused pins in the .xdc. On my set up, the number of critical warnings of this type seems to be capped at 100.
- When running synthesis/implementation/bitstream generation, use 8 tasks to speed up processing time (the ECE machines have like 20 cores).
- There are some specific switches you need to set, documented in the User Guide:
  - SW11, documented in table 1-2 (SoC configuration)
  - SW4, documented in table 1-11 (Programmable logic configuration)
    - We use a USB A to JTAG header connected to port J3 on the ZC706 and set SW4 to `10`