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| Tool Version : Vivado v.2018.2 (lin64) Build 2258646 Thu Jun 14 20:02:38 MDT 2018
| Date         : Sat Feb 23 18:00:41 2019
| Host         : ece023.ece.local.cmu.edu running 64-bit Red Hat Enterprise Linux
Server release 7.6 (Maipo)
| Command      : report_utilization -file test_unit_utilization_synth.rpt -pb
test_unit_utilization_synth.pb
| Design       : test_unit
| Device       : 7z045ffg900-2
| Design State : Synthesized
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Utilization Design Information

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1. Slice Logic
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+-------------------------+------+-------+-----------+-------+
|        Site Type        | Used | Fixed | Available | Util% |
+-------------------------+------+-------+-----------+-------+
| Slice LUTs*             |   89 |     0 |    218600 |  0.04 |
|   LUT as Logic          |   89 |     0 |    218600 |  0.04 |
|   LUT as Memory         |    0 |     0 |     70400 |  0.00 |
| Slice Registers         |   48 |     0 |    437200 |  0.01 |
|   Register as Flip Flop |   48 |     0 |    437200 |  0.01 |
|   Register as Latch     |    0 |     0 |    437200 |  0.00 |
| F7 Muxes                |    0 |     0 |    109300 |  0.00 |
| F8 Muxes                |    0 |     0 |     54650 |  0.00 |
+-------------------------+------+-------+-----------+-------+
* Warning! The Final LUT count, after physical optimizations and full implementation,
is typically lower. Run opt_design after synthesis, if not already completed, for a
more realistic count.


1.1 Summary of Registers by Type
--------------------------------

+-------+--------------+-------------+--------------+
| Total | Clock Enable | Synchronous | Asynchronous |
+-------+--------------+-------------+--------------+
| 0     |            _ |           - |            - |
| 0     |            _ |           - |          Set |
| 0     |            _ |           - |        Reset |
| 0     |            _ |         Set |            - |
| 0     |            _ |       Reset |            - |
| 0     |          Yes |           - |            - |
| 0     |          Yes |           - |          Set |
| 48    |          Yes |           - |        Reset |
```

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| 0     |          Yes |         Set |            - |
| 0     |          Yes |       Reset |            - |
+-------+--------------+-------------+--------------+
```

2. Memory

```
+----------------+------+-------+-----------+-------+
|    Site Type   | Used | Fixed | Available | Util% |
+----------------+------+-------+-----------+-------+
| Block RAM Tile |    0 |     0 |       545 |  0.00 |
|   RAMB36/FIFO* |    0 |     0 |       545 |  0.00 |
|   RAMB18       |    0 |     0 |      1090 |  0.00 |
+----------------+------+-------+-----------+-------+
```

* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E1

3. DSP

```
+----------------+------+-------+-----------+-------+
|    Site Type   | Used | Fixed | Available | Util% |
+----------------+------+-------+-----------+-------+
| DSPs           |    1 |     0 |       900 |  0.11 |
|   DSP48E1 only |    1 |       |           |       |
+----------------+------+-------+-----------+-------+
```

4. IO and GT Specific

```
+-----------------------------+------+-------+-----------+-------+
|          Site Type          | Used | Fixed | Available | Util% |
+-----------------------------+------+-------+-----------+-------+
| Bonded IOB                  |   96 |     0 |       362 | 26.52 |
| Bonded IPADs                |    0 |     0 |        50 |  0.00 |
| Bonded OPADs                |    0 |     0 |        32 |  0.00 |
| Bonded IOPADs               |    0 |     0 |       130 |  0.00 |
| PHY_CONTROL                 |    0 |     0 |         8 |  0.00 |
| PHASER_REF                  |    0 |     0 |         8 |  0.00 |
| OUT_FIFO                    |    0 |     0 |        32 |  0.00 |
| IN_FIFO                     |    0 |     0 |        32 |  0.00 |
| IDELAYCTRL                  |    0 |     0 |         8 |  0.00 |
| IBUFDS                      |    0 |     0 |       348 |  0.00 |
| GTXE2_COMMON                |    0 |     0 |         4 |  0.00 |
| GTXE2_CHANNEL               |    0 |     0 |        16 |  0.00 |
| PHASER_OUT/PHASER_OUT_PHY   |    0 |     0 |        32 |  0.00 |
| PHASER_IN/PHASER_IN_PHY     |    0 |     0 |        32 |  0.00 |
| IDELAYE2/IDELAYE2_FINEDELAY |    0 |     0 |       400 |  0.00 |
| ODELAYE2/ODELAYE2_FINEDELAY |    0 |     0 |       150 |  0.00 |
| IBUFDS_GTE2                 |    0 |     0 |         8 |  0.00 |
| ILOGIC                      |    0 |     0 |       362 |  0.00 |
| OLOGIC                      |    0 |     0 |       362 |  0.00 |
+-----------------------------+------+-------+-----------+-------+
```

5. Clocking

Site Type	Used	Fixed	Available	Util%
BUFGCTRL	1	0	32	3.13
BUFIO	0	0	32	0.00
MMCME2_ADV	0	0	8	0.00
PLLE2_ADV	0	0	8	0.00
BUFMRCE	0	0	16	0.00
BUFHCE	0	0	168	0.00
BUFR	0	0	32	0.00

6. Specific Feature

Site Type	Used	Fixed	Available	Util%
BSCANE2	0	0	4	0.00
CAPTUREE2	0	0	1	0.00
DNA_PORT	0	0	1	0.00
EFUSE_USR	0	0	1	0.00
FRAME_ECCE2	0	0	1	0.00
ICAPE2	0	0	2	0.00
PCIE_2_1	0	0	1	0.00
STARTUPE2	0	0	1	0.00
XADC	0	0	1	0.00

7. Primitives

Ref Name	Used	Functional Category
IBUF	75	IO
LUT6	51	LUT
FDCE	48	Flop & Latch
LUT5	29	LUT
OBUF	21	IO
LUT4	13	LUT
CARRY4	8	CarryLogic
LUT3	3	LUT
LUT1	2	LUT
LUT2	1	LUT
DSP48E1	1	Block Arithmetic
BUFG	1	Clock

8. Black Boxes

Ref Name	Used

9. Instantiated Netlists

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+----------+------+
| Ref Name | Used |
+----------+------+
```