# **Identity Checker with FPGA**

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# **Application Area**



#### Functionality

Facial Detection

Software+Hardware (FPGA)

**Facial Recognition** 

Software

**Areas** 

#### Why FPGA?

Significant parallelism in Image processing algorithms

# **Solution Approach - Overall**

Software



Laptop with Camera



Django Framework (webapp)



Viola-Jones Algorithm (detection)



Eigenface Algorithm (recognition)



Hardware

#### KC-705 FPGA Board



Viola-Jones Algorithm (detection)

# **Solution Approach - Facial Detection**



# **Solution Approach - Facial Recognition**



Yale Faces Database 15 subjects, 166 images

#### Training

- 1. Prepare a face database with 8 20x20 images per subject.
- 2. Use a set of eigenvectors to represent how each face differs from the mean face.
- The eigenvectors are called "eigenfaces". They measure the "variance" of the face database.

#### **Classification**

- Project new test image onto eigenfaces. This tells us how different the test image is from the mean face.
- 2. Find a face that differs the same way as the input image. That face is the closest match.

# **Block Diagram**



## **Complete Solution - Add Face**

#### **Identity Checker**



Check Identity

## **Identity Checker**

Enter your name for the Identity Checker:

Junye		
Chen		

Submit

#### **Identity Checker**















# **Complete Solution - Recognize Face**

#### **Identity Checker**

## Identity Checker

## **Identity Checker**









You must be:Junye Chen

Restart

# **Metrics and Validation - Correctness**



Yale Faces Database 15 subjects, 166 images

#### **Facial Detection**

#### **Facial Recognition**

- Goal: 80% accuracy
  - "box" the face if there is one
  - Reject if no face
- <u>166</u> images
- 163 Faces correct
- <u>98%</u> accuracy
- Good lighting

- Goal: 80% accuracy
  - Identify person's name, assuming face is in database
  - 163 images, 8\*15=120 training images
- <u>43</u> test images
- <u>37</u> correctly recognized
- <u>86%</u> accuracy

# **Metrics and Validation - Speedup**

Target: 0.05s (detect one face on software)

FPGA Baseline: 0.17s

Goal: 5x speedup

Optimization Step	Improvement	
Faster clock: 50MHz => 200MHz	0.17s => 0.0826s	
Loop pipeline	0.0826s => 0.037s	
Loop unroll	0.037s => 0.031s	

## Result: 1.6x speedup

## **Project Management**



## **Lessons Learned**

- Always have contingency plans
- Identify dependencies between tasks, and follow schedule closely
- Diversification of team members is very important