Design Review Presentation

Team C7

Application Area

- Facial detection + facial recognition on FPGA
- Areas:
  - Software systems
  - Hardware Systems
- Image processing algorithms have significant parallelism, and thus large potential for speedup

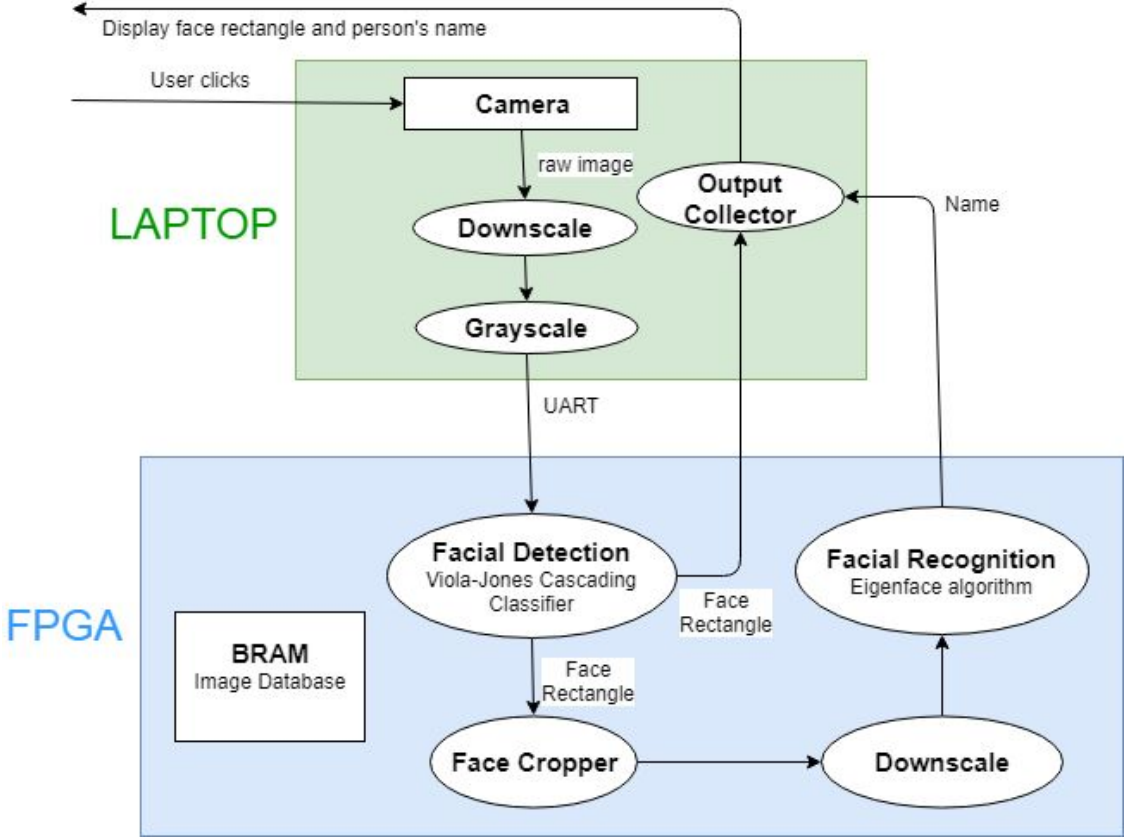
Solution Approach

- KC-705 FPGA Board (obtained from course hub)
- Laptop with Camera
- Viola-Jones algorithm vs Neural Net
- Eigenface algorithm

System Specification

1. Laptop
    - Easily take picture
    - Downscale + grayscale
2. UART Cable
    - Send picture pixel by pixel
3. Viola-Jones Cascading Classifier
    - Pass all subwindows through the classifier
    - Output the face rectangle
4. Face Cropping and Downsample
5. Eigenface Recognition

Block Diagram



Implementation Plan

- Laptop from us
- KC705 board from course inventory
- Vivado License from CMU
- UART module from Vivado
- Download pre-trained Viola-Jones weights
- Write Viola-Jones cascading classifier module
- Write Eigenface module

Metrics and Validation

1. Correctness
    - Add faces and recognize correctly at least 80% of the time.
2. Speedup
    - Measure software implementation using linux time command or timing functions in standard C.
    - Measure FPGA implementation in number of clock cycles.
    - Achieve at least 5x speedup in FPGA over the system on software.
    - I/O bottleneck
        - 160x120 image transfer
        - Assume 460800 bit/second, it takes about 160x120x8 / 460800 = 0.3s

Project Management - Work Distribution

- Sheng-Hao - Hardware / FPGA
  - Re-acquaint with Vivado and shows Hans how to use it
  - Work with Hans to convert algorithms to RTL and optimize them
- Hans - ML / Algorithms
  - Implement Viola-Jones cascading classifier in C
  - Implement Eigenface algorithm in C
- Andy - Software / App
  - Design the app interface
  - Preprocess image (B&W, scale down, etc.)
  - Create a local or cloud database to keep track of face data

Project Management - Rough Deadlines

Task	Deadline
Viola-Jones Cascading Classifier in C, UART Setup	3/3
Viola-Jones testing	3/7
Viola-Jones on FPGA	3/17
Test face detection only on FPGA	3/24
Eigenface Recognition in C	3/31
Eigenface testing	4/7
Eigenface Recognition on FPGA	4/14
Integration test	4/21

Project Management - Gantt Chart