Title: TEAM STATUS

Team B2 - Eshani Mishra (emishra), Kimberly Lim (klimjinx), Shruti Narayan (shrutin1)

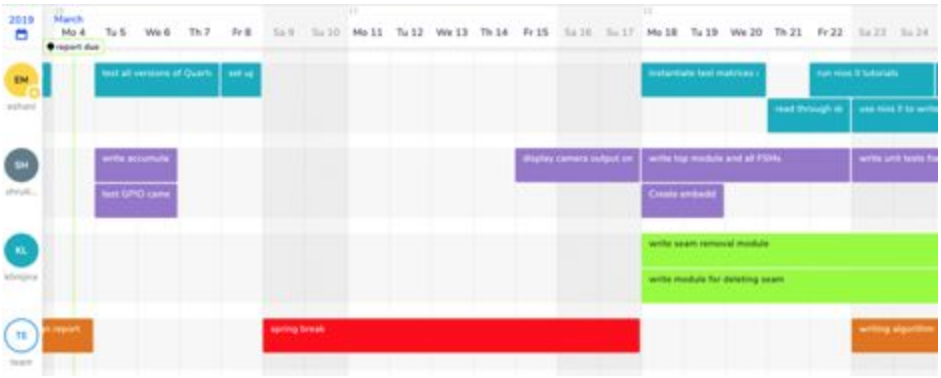
What are the most significant risks that could jeopardize the success of the project? How are these risks being managed? What contingency plans are ready?

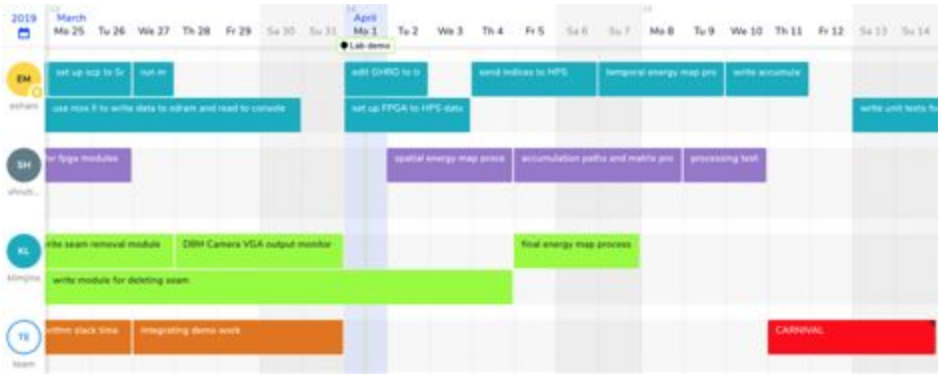
- Figuring out how to interface between the HPS and the FPGA (specifically, how to switch control between the C code on Nios and the Verilog in Quartus) has proven to be a challenge.
    - Risks Managed: Our TA has given us resources to reference on how the qsys module is instantiated… This will give us understanding to follow the same method in our code
    - Contingency: We use the full VHDL/Verilog demo that we had for the mid-semester. It will introduce complications with pre and post processing of the video frame data, that in turn might make parallelization difficult and extend our time.
- Previously we discussed a choice between the Linux console version and the Linux GUI version to use on the board - we chose to work with the console version for familiarity and simplicity. However, we found that necessary C++ libraries not available on the Linux console version.
    - Risks Managed: We will switch to using the GUI version. Problems with this is how we will deal with two VGA outputs (GUI and the video output itself) We might write something to handle switching between displays
    - Contingency: We will write the C++ portion of code without extra libraries

Were any changes made to the existing design of the system (requirements, block diagram, system spec, etc)? Why was this change necessary, what costs does the change incur, and how will these costs be mitigated going forward?

- We changed our schedule (removed slack time) to account for extra time spent on unexpected issues (ethernet, understanding demo code, etc). We still have time to achieve what we intended to.

Provide an updated schedule if changes have occurred.


2019
March
Mo 4
Tu 5
We 6
Th 7
Fr 8
Mo 11
Tu 12
We 13
Th 14
Fr 15
Mo 18
Tu 19
We 20
Th 21
Fr 22
report due
EM
eshani
SH
KL
klimjinx
TE
team
write accumula
write seam removal module
write module for deleting seam
spring break


2019
March
Mo 25
Tu 26
We 27
Th 28
Fr 29
April
Mo 1
Tu 2
We 3
Th 4
Fr 5
Mo 8
Tu 9
We 10
Th 11
Fr 12
Lab demo
EM
eshani
SH
KL
klimjinx
TE
team
write seam removal module
DBM Camera VGA output monitor
final energy map process
write module for deleting seam
CARNIVAL


2019
April
Mo 15
Tu 16
We 17
Th 18
Fr 19
Mo 22
Tu 23
We 24
Th 25
Fr 26
in lab demo
EM
eshani
design user pol
conduct user testing
design interfac
SH
shruti...
return pixel processing
No work
calcul
design interfac
KL
klimjinx
calculate benchmark metrics
calculate qualit
get results of user testing
TE
team
running unit tes
final testing
poster and final demo preparation