Title: TEAM STATUS

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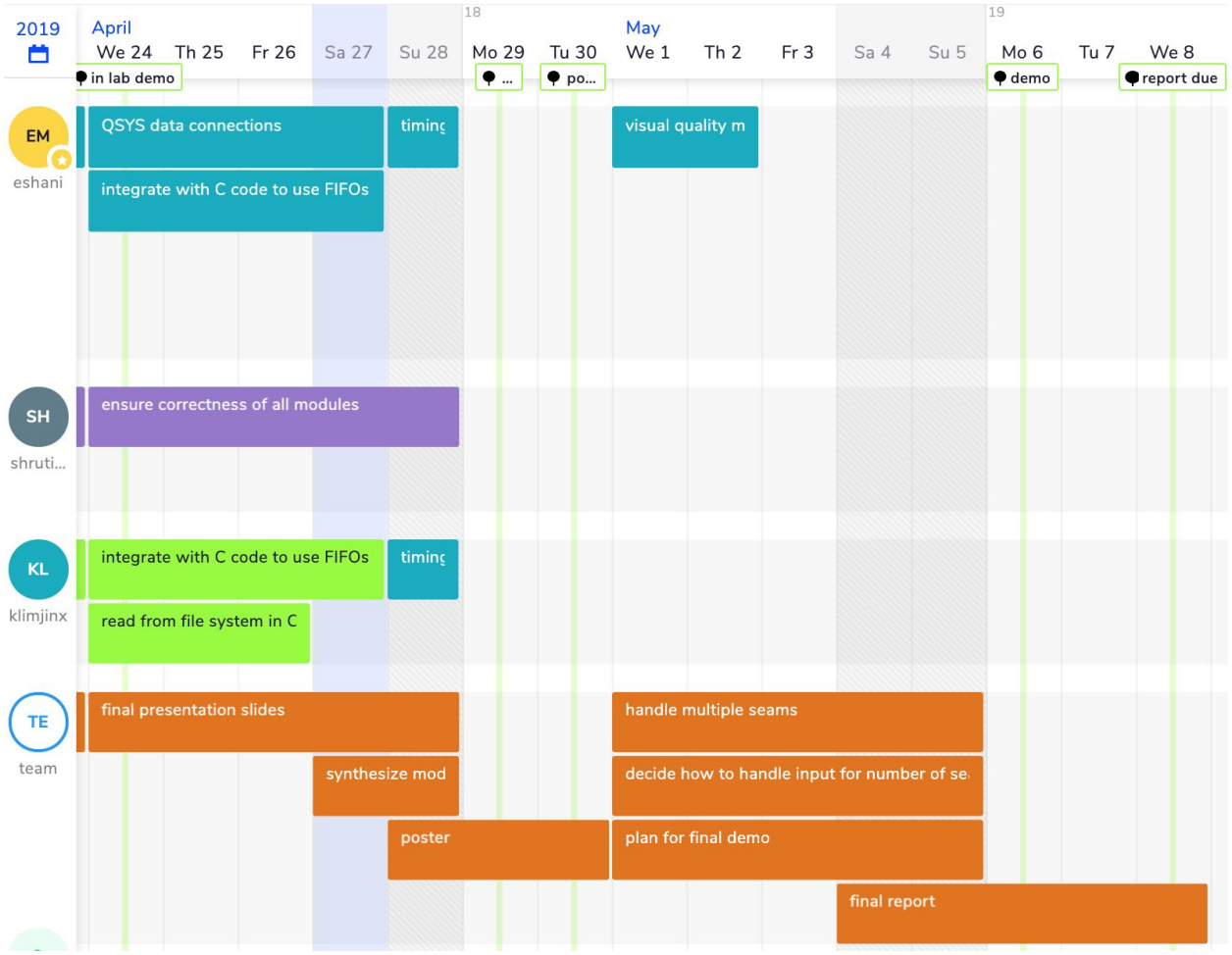
What are the most significant risks that could jeopardize the success of the project? How are these risks being managed? What contingency plans are ready?

- Transition from simulation to synthesis - we have to integrate the data FIFO with the the algorithm on the board and there could the be issues due to timing and transitioning from using simulation models of embedded memory to M10K block on the board
    - We have tried to manage this risk by ensuring correctness of the algorithm through simulation so bugs are reduced when synthesizing
- Display for DEMO - We have to decide if displaying the video on the Linux filesystem GUI on our fpga would work as a viable display for our final demo
- Timing metrics - We have to determine if the energy map computation or the seam removal on the SoC will be more time consuming
    - Since the video is getting smaller for each iteration, both the energy map computation and seam removal should be shorter for each seam
    - Since the seam removal on the SoC is limited by the clock speed of the processor which cannot be controlled and the removal could be much faster on another processor, so our main focus is to optimize the algorithm

Were any changes made to the existing design of the system (requirements, block diagram, system spec, etc)? Why was this change necessary, what costs does the change incur, and how will these costs be mitigated going forward?

- Decided to use HPS to read video data from Linux file system and send to FPGA using a FIFO queue instead of the camera input because the read and writes to SDRAM were clocked differently and this was causing the writes to memory and display values to become garbled when we made changes to the code
    - We decided to move away from the camera
- Made minor changes the our embedded memory blocks to optimize energy map computation

Provide an updated schedule if changes have occurred.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