Title: TEAM STATUS

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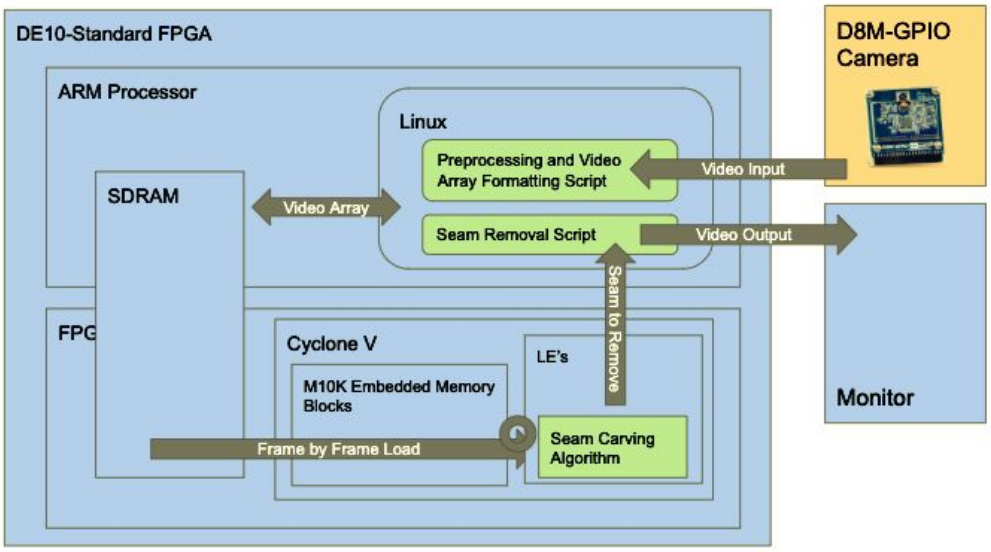
What are the most significant risks that could jeopardize the success of the project? How are these risks being managed? What contingency plans are ready?

- Demo Detour
    - Did not account for the tasks needed for the demo:
        - Mapped out requirements for demo after discussion with Professor and TA
    - Luckily, we had slack time and used it for this

Were any changes made to the existing design of the system (requirements, block diagram, system spec, etc)? Why was this change necessary, what costs does the change incur, and how will these costs be mitigated going forward?

The block diagram is a little different from the one presented. Firstly, the SDRAM is actually shared between ARM and FPGA. We can now remove the step of data transfer between the 2 SDRAMs before. Secondly, we are going to transfer directly to the logic elements in the FPGA instead of loading first into the memory blocks to improve performance. We will have to redesign some block diagrams, but this is small and were anticipated beforehand.



Provide an updated schedule if changes have occurred

No changes