

Title: TEAM STATUS

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What are the most significant risks that could jeopardize the success of the project? How are these risks being managed? What contingency plans are ready?

- Handling overlapping seams in 5 seam removal, could cause issues if we try to remove the same pixel twice
 - Contingency plan: searching for duplicates in the pixel indices that are sent to the SoC and removing only the path of minimum accumulated value that includes the duplicated pixel
- Requiring software that runs on windows for video metrics and system interconnect in the DE-10
 - Changed our assigned space to a lab room with PCs running Windows
 - use customized install with help from ITS

Were any changes made to the existing design of the system (requirements, block diagram, system spec, etc)? Why was this change necessary, what costs does the change incur, and how will these costs be mitigated going forward?

- We added an additional post-processing step on the SoC: searching for duplicates in the pixel indices that are sent to the SoC and removing only the path of minimum accumulated value that includes the duplicated pixel
- Processing data as it is received in FPGA vs storing data in FPGA's embedded memory first and then processing it: We are currently debating two options for loading data into the FPGA from the HPS. The first option involves loading the data serially from the HPS to the FPGA and then putting it in embedded memory immediately. After that we would proceed with the algorithm with the optimization of parallelizing by row as previously planned. The other option would be to process the data immediately after serially transferring data through the HPS to the FPGA. The first option would speed up the algorithm itself, but add extra time for serial data transmission and set up, The second option would save time by combining transmission and processing but would force the processing to be serial.

Provide an updated schedule if changes have occurred.



