Shruti Narayan (Team B2)

- What did you personally accomplish this week on the project? Give files or photos that demonstrate your progress. Prove to the reader that you put sufficient effort into the project over the course of the week (12+ hours).
 - Identified further bottlenecks in algorithm and discussed with group on how to handle them (double buffering for frame loading, how to remove seams and reorganize video array representation)
 - Researched project feasibility on DE0-CV and DE2-115 boards (focusing on memory organization and allocation as well as external device interfacing)
 - Concluded it is feasible and the best option to be able to achieve what we want (focus on algorithm and less on interfacing with external devices to fpga)
 - Researched cameras and other external devices necessary
 - Debated between two viable options (D8M-GPIO and TRDB-D5M) and settled on D8M-GPIO for video capability and detailed documentation
 - Read the full seam carving algorithm in detail for clarity
- Is your progress on schedule or behind? If you are behind, what actions will be taken to catch up to the project schedule?
 - Progress is slightly behind we aimed to have the module designs well in progress but had to spend time discussing potential design bottlenecks and reconsider the technology to be bought
 - Since we have to spend unforeseen time testing out the camera to finalize our fpga choice, we will still be a bit behind next week. However we have accounted for slack time now
 - Next week I and the rest of the team will spend extra time on the design and aim to complete fsm design and more generalized block diagrams before the weekend
- What deliverables do you hope to complete in the next week?
 - Next week we plan to experiment with the camera and ensure it works. My goal is to have a camera demo working (go from taking a video to processing on FPGA to displaying as is on a monitor)
 - We also will determine if the camera imaging kit will allow for the necessary modifications
 - The later half of the week should also yield the module designs, ready for team review and finalizing before the design presentation