Title: TEAM STATUS

Team B2 - Eshani Mishra (emishra), Kimberly Lim (klimjinx), Shruti Narayan (shrutin1)

What are the most significant risks that could jeopardize the success of the project? How are these risks being managed? What contingency plans are ready?

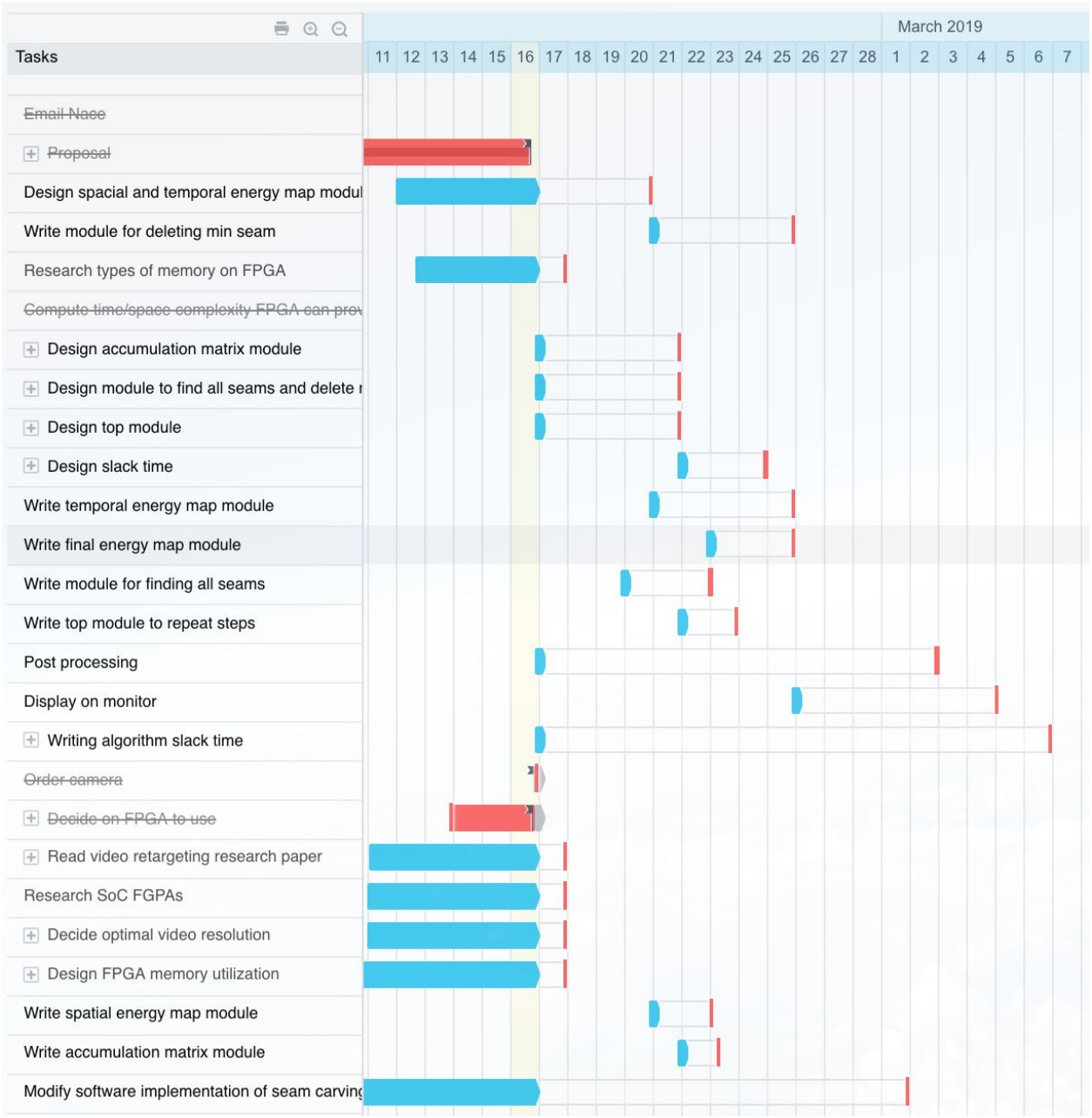
- Memory constraint of the FPGA
    - Why?
        - We set down and discussed the seam-carving algorithm further together. Some approaches would be near impossible due to the amount of memory the algorithm would incur
            - Block ram cannot hold a full 3D voxel cube
            - We are bounded by the amount of memory for program execution
    - Contingency Plan (in order of preference)
        - SOC solution: solves preprocessing constraints
            - The DE10 board has a system on chip - we would be able to run Linux and handle all the preprocessing and postprocessing of the video on this
            - It will also simplify the interfacing between multiple components (FPGA and external memory)
            - Has 5,761 Kbits embedded memory compared to 3080k embedded memory on De2115 FPGA
            - Could be used to divide video into blocks manageable by FPGA memory and sent in intervals
        - Constrain video resolution and fps
            - Gifs are 12 fps and are of lower resolution
            - Gifs are popular in instant messaging apps
            - Smaller .gifs mean faster upload/downloads speeds for those with bad internet connection
        - Xilinx Board (Zynq)
            - Team D9's project is similar with ours. They have chosen to use a Xilinx board for their project mainly due to the larger memory. We will migrate to use this board if needed

Were any changes made to the existing design of the system (requirements, block diagram, system spec, etc)? Why was this change necessary, what costs does the change incur, and how will these costs be mitigated going forward?

- Purchased 8 Mega Pixel Digital Camera Package with GPIO interface (FPGA Camera)
    - Contains MIPI camera module, MIPI decoder, camera capture and display reference design
    - The MIPI camera module captures images and sends them out in a MIPI video signal package

    - Compatible with 240, 341 and Altera-SoC FPGA board listed in Canvas pdf of available boards
    - Necessary to avoid the extra time spent preprocessing and postprocessing our videos from scratch
    - This cost is a not a huge add to our budget which was under utilized
    - https://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=68&No=1011&PartNo=1
- Discussion to pair up with domain expert
    - Professor Low Tze Meng has experience with image and video processing, particularly the seam-carving algorithm. He also works with FPGAs and performant C code. We discussed with Professor Nace and Professor Low about this new approach in 18-500 where teams are paired with a domain expert and we are very interested in it
- Lower resolution for input video
    - We wanted to be able to store the matrices for the spatial and temporal energy maps within the board's embedded RAM
    - Requires enough space for 4 video frames to be stored at once

Provide an updated schedule if changes have occurred.


March 2019
Tasks
11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 1 2 3 4 5 6 7
Email Nace
Proposal
Design spacial and temporal energy map modul
Write module for deleting min seam
Research types of memory on FPGA
Compute time/space complexity FPGA can prov
Design accumulation matrix module
Design module to find all seams and delete r
Design top module
Design slack time
Write temporal energy map module
Write final energy map module
Write module for finding all seams
Write top module to repeat steps
Post processing
Display on monitor
Writing algorithm slack time
Order camera
Decide on FPGA to use
Read video retargeting research paper
Research SoC FGPAs
Decide optimal video resolution
Design FPGA memory utilization
Write spatial energy map module
Write accumulation matrix module
Modify software implementation of seam carving

Kimberly Lim (Team B2)

What did you personally accomplish this week on the project? Give files or photos that demonstrate your progress. Prove to the reader that you put sufficient effort into the project over the course of the week (12+ hours).

- Modified Open-Source .cpp implementation of seam carving for video seam carving
    - The optimal seam for one frame is achieved by finding the minimum cut on the seam cube which consists of the current frame and the next 4 frames. We phrase this a **5 Frame Look-Ahead Cut**
    - This is just one approach of the seam-carving algorithm for video. Part of our project is to determine the best modification of seam-carving for video that fits our constraints
- Added documentation for environment setup for the rest of my team members
- Updated .cpp libraries for OpenCV 4.x compatibility
- Added benchmarking code for runtime and cpu cycles
- Ran some preliminary benchmarks for video seam carving (graph cut with 5 frame look ahead energy).
    - To remove 10 vertical and 10 horizontal seams using 8 threads:
        - Program time: 202.94 seconds
        - Program cycles: 3285536764 cycles
        - Source Video: https://github.com/kimberlyljx/fpga-seam-carving/blob/master/parallel-video-retargeting/realshort.mp4
        - Result Video: https://github.com/kimberlyljx/fpga-seam-carving/blob/master/parallel-video-retargeting/realshort-result.mov
- Setup git repository that contains aforementioned code: https://github.com/kimberlyljx/fpga-seam-carving
- Discussed with team members on FPGA imaging kit purchase and model selection
- Discussed with team D9, Professor Nace, Professor Low and Professor Mukherjee about pairing up with domain expert for project
- Attended Professor Low's lecture on Monday, Feb 11

Is your progress on schedule or behind? If you are behind, what actions will be taken to catch up to the project schedule?

- Behind schedule for FPGA code design
    - We anticipated in our initial schedule and had designed for some slack
    - We updated our old Gantt schedule to reflect this
    - Setup a meeting on Sunday for task completion

What deliverables do you hope to complete in the next week?

- Create block diagrams for FPGA module design

- Design finite state machine for input-output behavior
- Finish .cpp implementation for **Static Seam Removal** approach of seam carving