

What did you personally accomplish this week on the project?

- SoC research
 - Learned shared memory management and FPGA to processor communication on Intel SoCs through resources on Intel and Terasic's websites

DE2-115 (240 board)	DE10 (SoC)
<ul style="list-style-type: none"> ● 128 MB SDRAM (enough to store entire 5 s video sample at 360p 30fps) ● well documented examples ● Compatible with terasic imaging kit ● Cannot handle preprocessing, will have to use ethernet connection if inputting videos through imaging kit is not viable ● Integrated 10/100/1000 mbps Ethernet ● 3,888 Kbits embedded memory 	<ul style="list-style-type: none"> ● 64 MB SDRAM (enough to store entire 5 s video sample at 360p 30fps) ● Difficult to find tutorials/resources other than those provided by terasic ● Compatible with terasic imaging kit ● HPS able to handle preprocessing ● High bandwidth interconnect between FPGA and ARM processor (up to 125 Gbps) <ul style="list-style-type: none"> ○ Much faster than ethernet communication ● Linux image provided ● Automatic generation of interconnect logic through Quartus ● 5,761 Kbits embedded memory

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- Researching alternate methods of communication between FPGA and Pi
 - Sending video data through SPI/UART is not viable
 - Learned Ethernet capabilities of DE2-115 and DE10-Standard
- Read research paper on seam carving - http://www.eng.tau.ac.il/~avidan/papers/vidret.pdf?fbclid=IwAR2QiB0f6tUhrd0ejbnuwE9qnuEyjSX_9q7XsL-Bs3GO9uLfhJb5eIHWgOo
- Updated task list and Gantt chart on Bitrix (updated Gantt chart is in team page)
 - Fixed start dates as recommended in proposal presentation feed
 - Added new tasks for additional research that was required to select the correct FPGA to use and whether SoC was required
 - Pushed back deadlines for FPGA module design due to additional research time
- Reserved space for room/bin
- Created Terasic account to view shipping options for FPGA camera module and submitted purchase request

Is your progress on schedule or behind? If you are behind, what actions will be taken to catch up to the project schedule?

- We are behind on FPGA module design due to some additional planning and research we had to do to manage preprocessing and memory management
 - We plan on getting the majority of our design planned out on on the 17th and completing our design the following week
 - We have updated our Gantt chart to reflect the changes

What deliverables do you hope to complete in the next week?

- FPGA module design (FSMs) for fpga implementation of seam carving algorithm
- Use terasic imaging kit with de2115 and test VGA display of video

- Finish FPGA memory management design