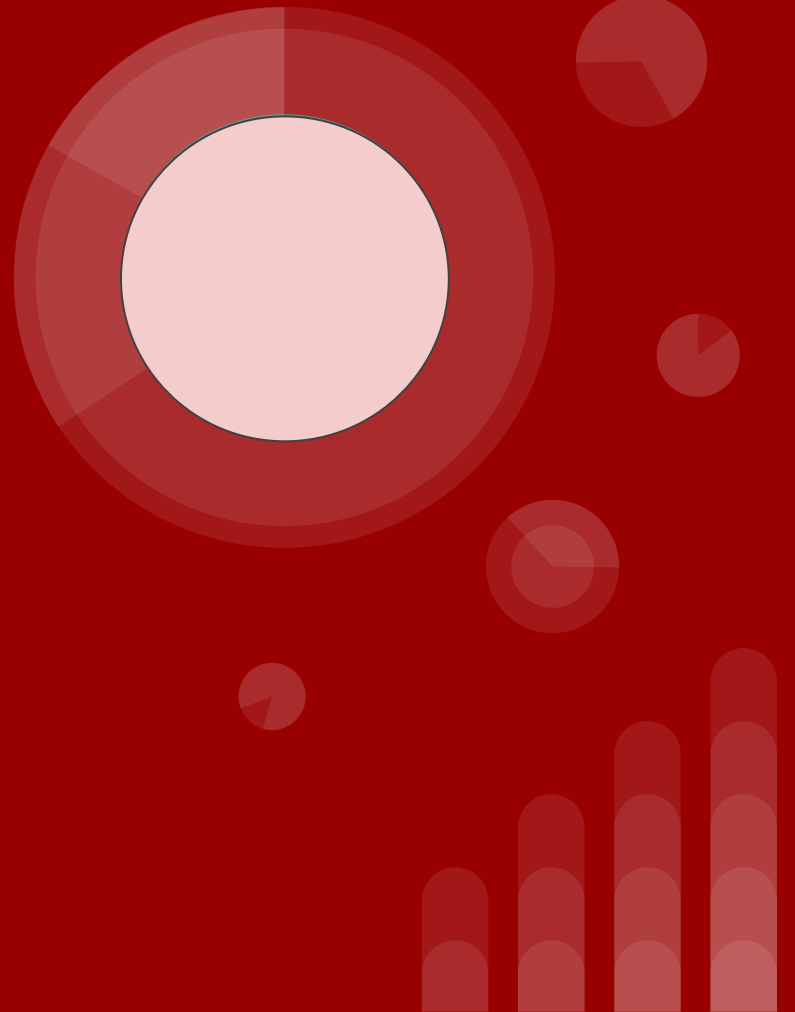


FPGA Accelerated Seam Carving for Video

A Design Overview

B2: Kimberly Lim, Eshani Mishra, Shruti Narayan



Application Area



Content-aware re-scaling intelligently targets parts of the frame to remove.

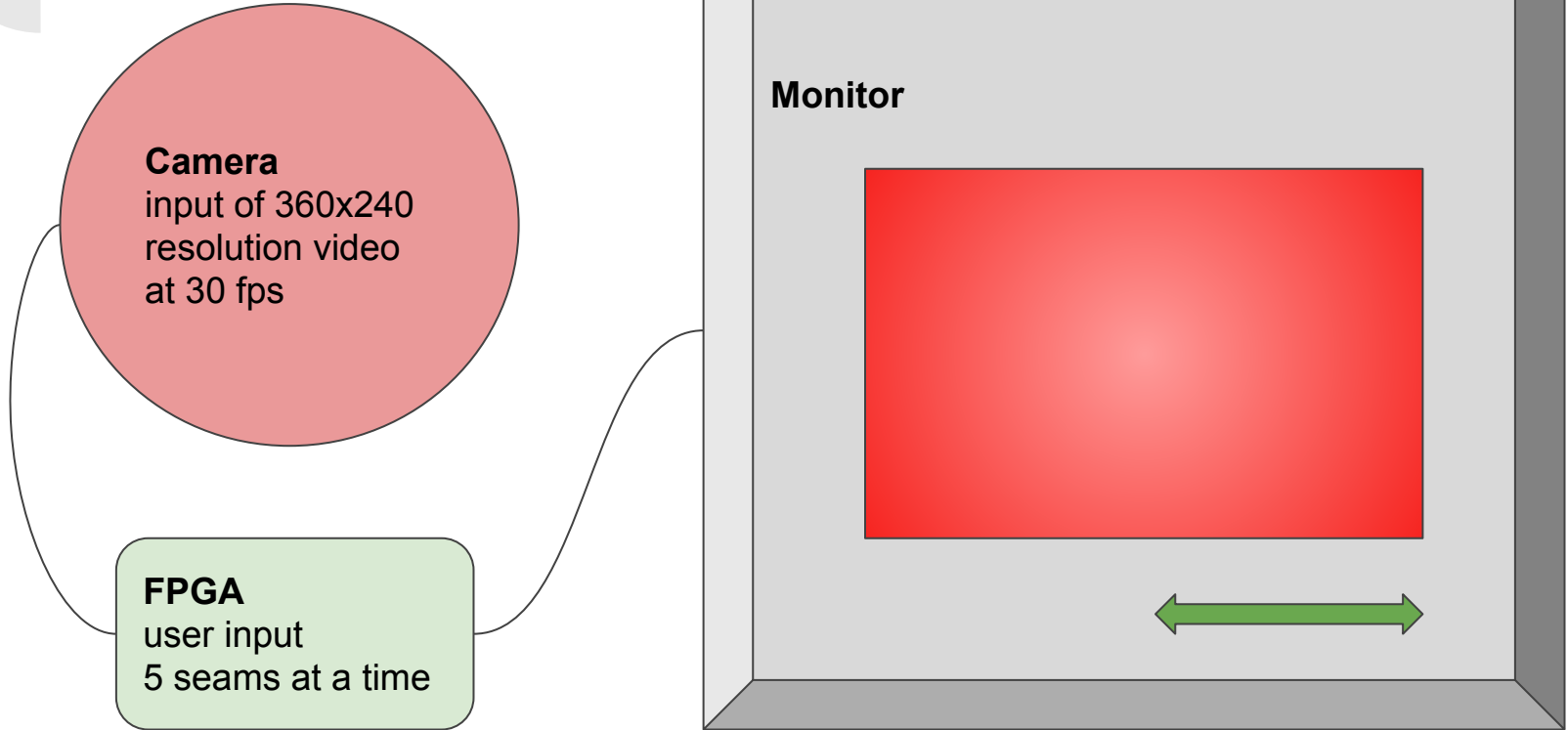
- Reduced video size (users often run out of space)
 - Carve out unwanted pixels and save what's important
- Draw attention to important aspects of video
 - Highlight important aspects by removing unwanted seams
- Video processing is often slow
 - FPGA for Acceleration

Application Area

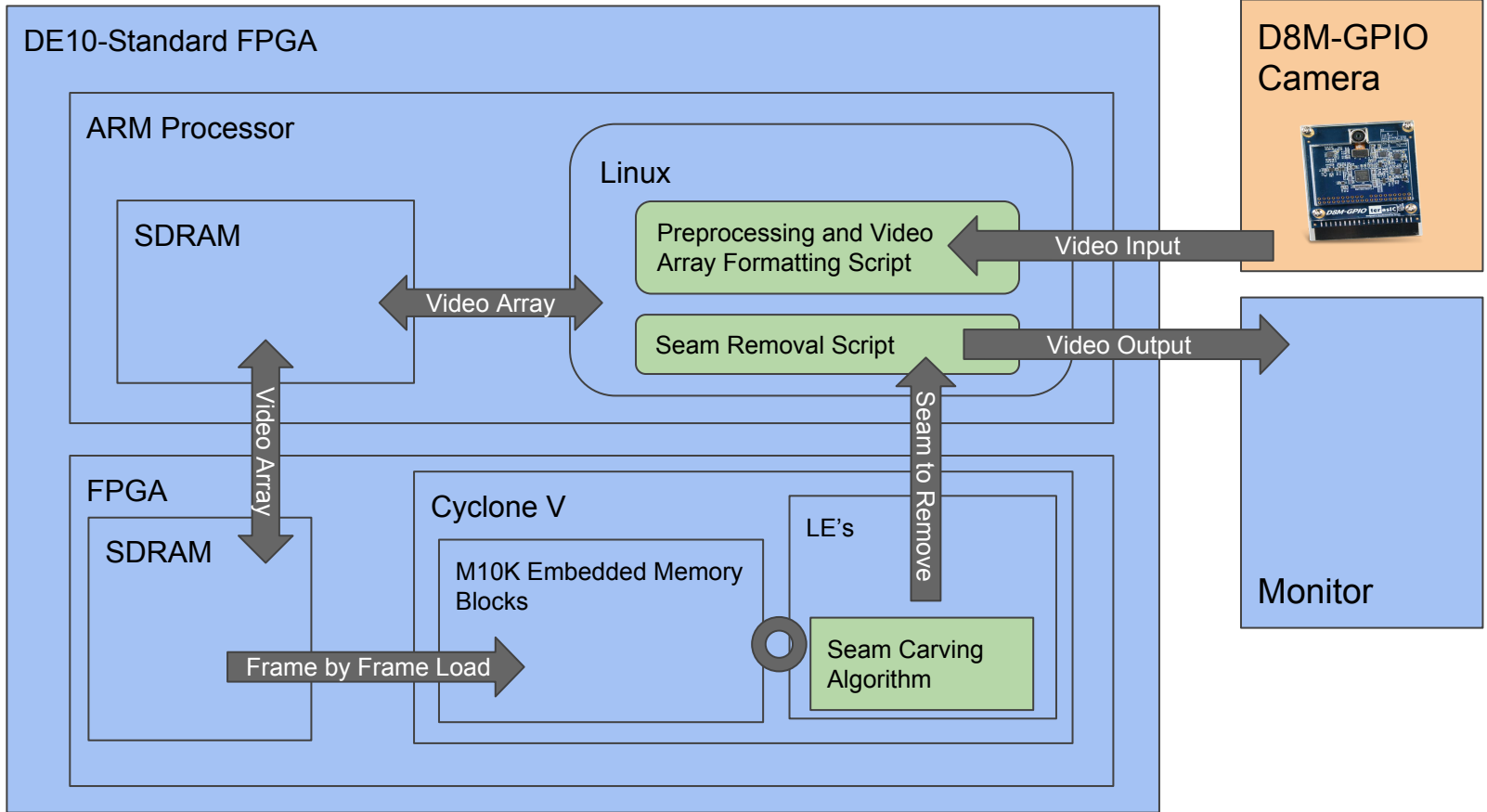
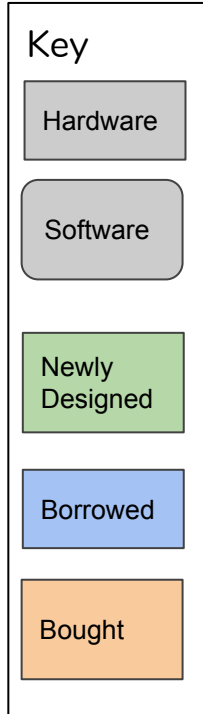


Naive implementation of restitching of seam-carved images shown on left (spatial only). Static seam carving on right uses temporal and spatial so less distortion. Computational complexity becomes the *bottleneck* of the implementation of the algorithm. A hardware-oriented seam carving algorithm using FPGA is proposed to improve performance.

Overview of MVP



Block Diagram: Data Transfer through Hardware



Algorithm Overview

Stage 1

Stage 2

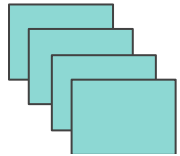
Stage 3

-1	0	+1
-2	0	+2
-1	0	+1

x filter

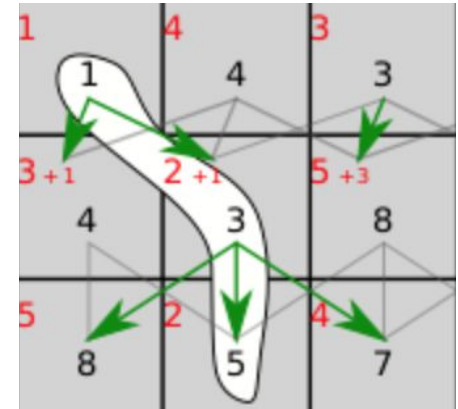
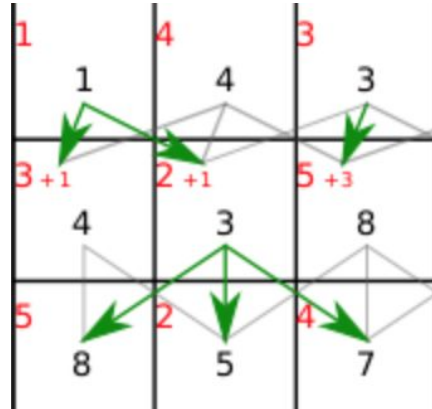
+1	+2	+1
0	0	0
-1	-2	-1

y filter



1	2	3
5	6	7
9	10	11

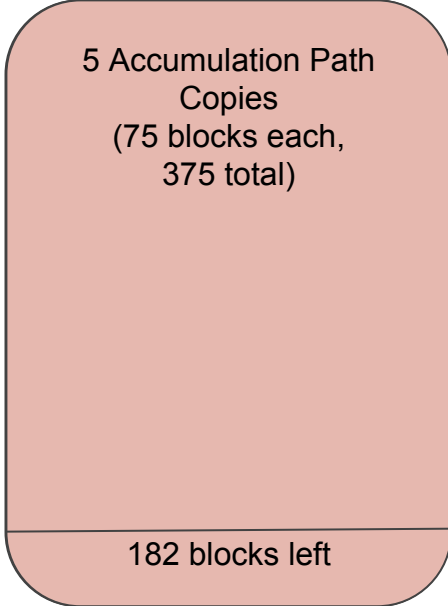
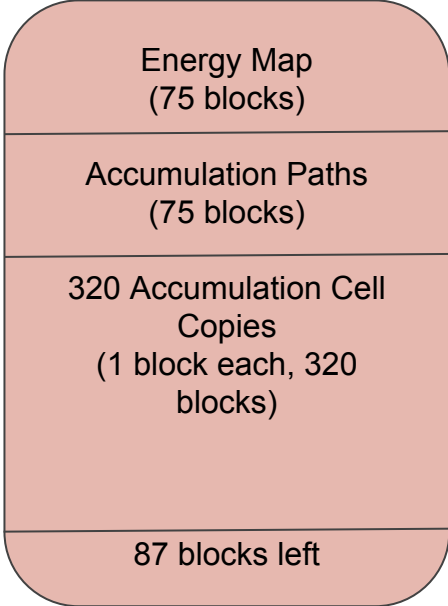
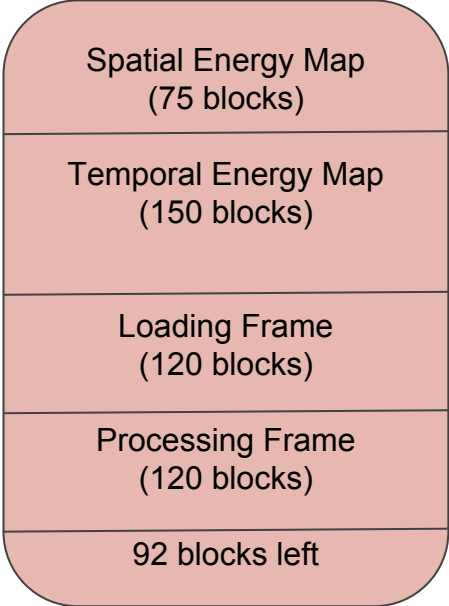
$$E_{\text{temporal}}(i, j) = \max_{t=1}^N \left\{ \left| \frac{\partial}{\partial t} I_t(i, j) \right| \right\}$$



Memory Allocation in FPGA



5
5
7
M
1
0
K



Algorithm Implementation

Stage 1

Stage 2

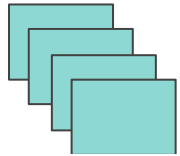
Stage 3

-1	0	+1
-2	0	+2
-1	0	+1

x filter

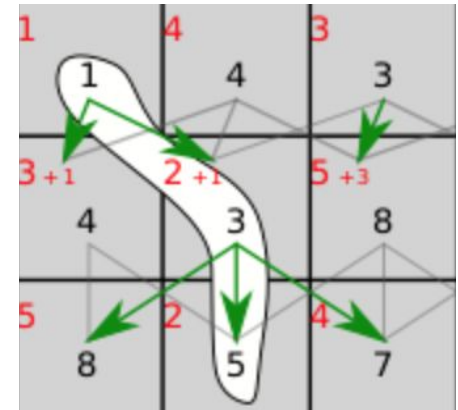
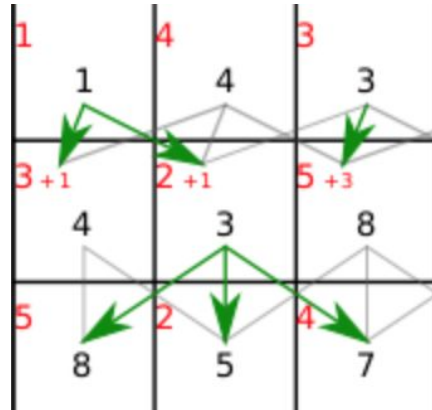
+1	+2	+1
0	0	0
-1	-2	-1

y filter



1	2	3
5	6	7
9	10	11

$$E_{\text{temporal}}(i, j) = \max_{t=1}^N \left\{ \left| \frac{\partial}{\partial t} I_t(i, j) \right| \right\}$$



Metrics and Validation

01	Timing	<ul style="list-style-type: none">• Compare against benchmark C++ implementation of seam carving• Goal: 5x speedup
02	Video Quality	<ul style="list-style-type: none">• PSNR, Spatio-temporal SSIM• User testing• Goal: <10% error compared to results from C++ implementation
03	Risk Factors/Unknowns	<ul style="list-style-type: none">• Remove less seams at a time (<5)• Change blocking to optimize parallelization• Memory consumption + timing analysis for test matrices using Quartus

Benchmark Analysis (360x240 at 30 fps with 1.4 GHz Intel Core i5)

Seams



- 30 vertical seams

Time



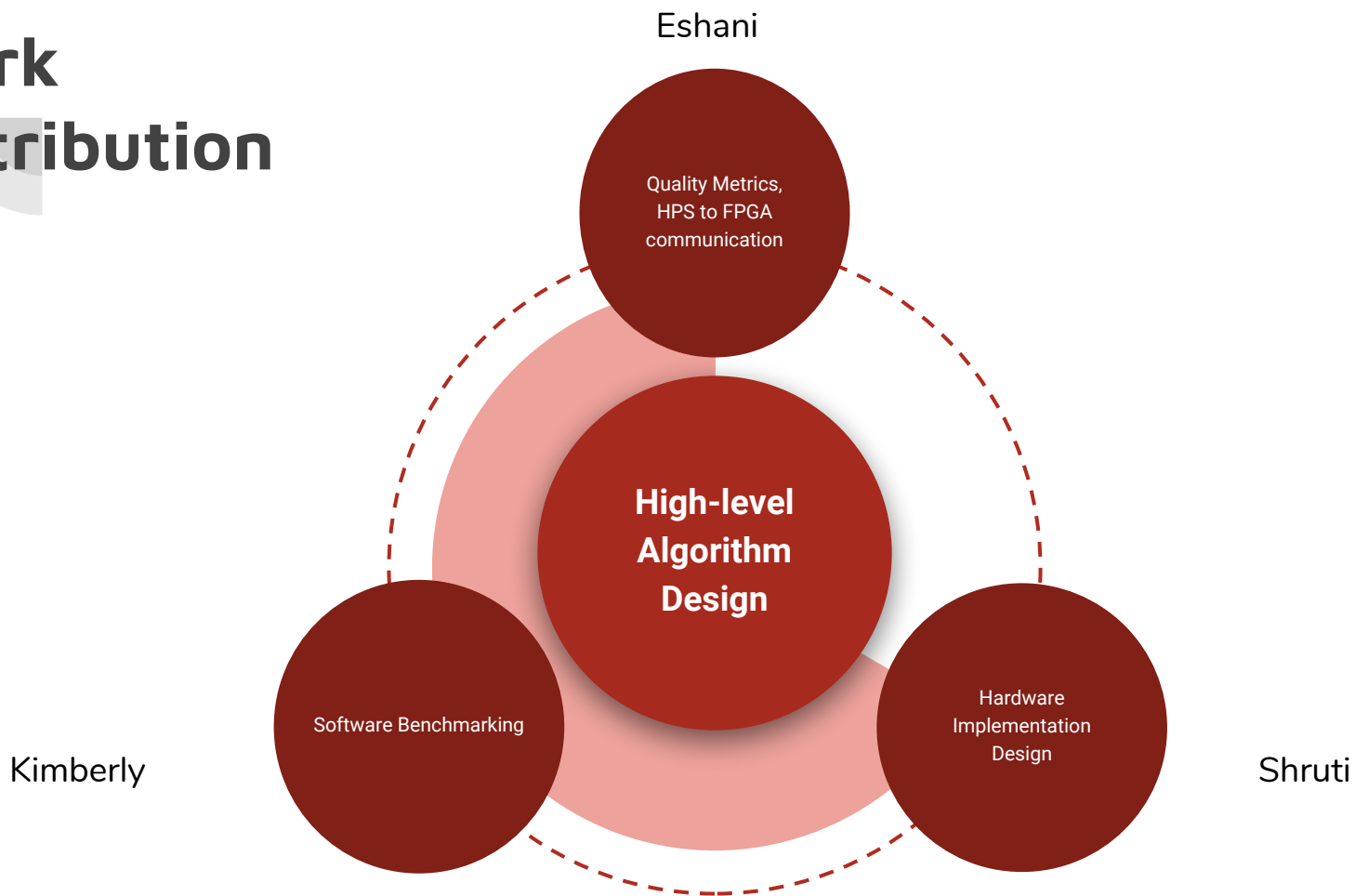
- 10.646925 seconds

Cycles



- 132360837 cycles

Work Distribution



Schedule



Ongoing and future tasks up until spring break.

(Post spring break for slack time as well as adding planned extension steps)

