Project Status Report #9
Group A3
4/20/19

This week we worked a lot on making sure our parts are ready to work with each other. The floating point unit has been improved for performance and is near ready for integration. We will be able to fully support the risc-v F extension. We don't have any stats for the FPU yet but should have some within the week. We took a closer at the vector extension and realized that there is a lot in the extension spec that we don't need to implement (or that we won't be able to support). The instructions that work with two different register files as well as the widening instructions are not necessary for what we need our core to accomplish.

The core's timing has been improved. We've added an AXI interconnect to the core and added the core to the Vivado IP integrator.

This past week we finally got the assembler working. We successfully got it to spit out some instructions correctly. We are modifying it to make sure it complies with what we want from the vector extension.