Project Status Report #8
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This week I worked on the memory interconnect for my coprocessor, which would connect over AXI to the supervisor core. This required a lot more work than I was originally thinking, since the memory switch to allow two master to talk to the block ram required a significant modification to my flow control model. This was because the memory switch was purely combinational, rather than being an extra register stage, since the instruction memory latency is a big issue for IPC.

I also had another issue I found with the fetch stage regarding the production of output values, but it only appears when the instruction memory and the instruction command pipelines are of different lengths, which is something I can completely avoid but is an issue I would like to run down later.

I also started work on the AXI infrastructure I needed to communicate with the coprocessor, which I can also leverage later for the some of the support IP that allows more efficient communication between the individual cores.