Cyril Agbi Capstone: Team A3

LOG: 4/14/19 –4/20/19

Worked on pipelining the floating point operation units. They are split up so that the exponent resolution, mantissa resolution, normalization and rounding in different stages. Divide and square root do their loops through a register to save time of doing 20-some adds/subtracts in a cycle. This also saves space since we don't need 20-some different mantissa resolution stages for those 2 operations. I have the decode logic for the FPU completed. I'm still strugging with a better way to implement the multiply-add instructions. For now, I am content with the way it currently works.

Me and David are still working on the integration. We went over some of the vector extension spec and decided on what parts of the spec we didn't need or were too excessive to include. We are working with Alex to make sure that the assembler is aware of the instructions that we do support.