

LOG: 3/31/19 –4/6/19

This week I started to work on integrating the FPU with the RISC-V core. David and I discussed the architecture (the pipeline) for the FPU. In our FPU pipeline, we have the following stages: Decode, execute, writeback, and rounding. The decode stage takes in an instruction that's part of the rv32 "F" spec and decides on which components to use. The execute stage contains all of the FP modules (add, multiply, sqrt, int2float, etc.). The writeback stage will provide a stage to resolve the output. Finally, the rounding stage will handle the rounding (if required).

So far, I have everything except the writeback stage and part of the decode stage implemented. I may need to make more stages since I am slowly adding instructions from the floating point spec. I should have this completed by this week. After this, we should be able to synthesize our design (checking how many resources it uses) and test it with the risc-v core.