Team Status Report #6
Group A3
3/30/19

This week our team worked on preparing for both integration of the FPU with the CPU implementation, as well as getting the vector assembler to compile instructions. For the CPU the focus was on a slight increase in IPC from the original of about 0.4 to now about 0.68, which will hopefully allow the CPU to better utilize the FPU during normal program operation. The CPU is a little harder to design than a traditional five-stage RISC design, in part because of arbitrary latency execution units like the FPU, but hopefully will be able to utilize them better than a traditional five-stage as well.

The CPU pipeline was given full register tagging as well this week, so that the FPU can be added to the design more easily, and better utilize it rather than having to wait constantly for write-after-write conflicts. We also focused on some floating point conversion functions that we will need to bring data in and out of the floating point unit, and that we need to have written tests for, at least before final integration.

The vector assembler is falling behind schedule right now, as we were hoping to have it generate instructions a couple weeks ago, and instead move onto other software objectives while we tried to get hardware working that could run those instructions. Hopefully the work we already put in is close to functional, but this is uncertain right now.