Team Status Report #5
Group A3
3/23/19

This week our group got our CPU working, by passing both the RISC-V tests but also running C code that we compiled for it, which could use the ECALL instruction to emulate character printing in simulation. The CPU also synthesizes properly to the FPGA, with less than 1000 registers, which is very acceptable for our CPU design, since with that usage we are going to run out of DSP slices for our FPU way earlier.

Our floating point logic also works for all of the operations we need to support, aside from only ever being off in the least significant bit in a small number of cases. We are trying to fix this, but are going to be integrating the logic into our CPU next, and if necessary this is an acceptable level of imprecision.

We are still working on getting the GCC assembler to generate the vector instructions that we need to support in RISC-V, but it is mostly just trying to get through the build process right now, and we think that we are not that far away from getting the assembled instructions to generate.