Project Status Report #4
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This week I worked on finishing the design report document, as well as working out some more of the design for the main CPU core we are using. First, in the design report I had to think through some more of the memory hierarchy, which we had previously not really thought through as carefully. I also did some research on what kind of benchmarks we could use for the architecture and came up with some better targets for what we could do for mandelbrot, ray-tracing, or deferred rendering.

Working on the CPU I started work on the system module for handling control/status registers. I also test-benched the writeback module and fixed a bug in my flow control logic. I am currently writing out the execute logic for the CPU.

To help for final FPU integration I also elaborated its block-diagram, with some of the later stages of each FPU operation being shared between multiplication, division, etc, rather than each having its own rounding module. The rounding logic could accept a single result each cycle, so forcing all the different operations to share it does not pose a bottleneck.