Project Status Report #3
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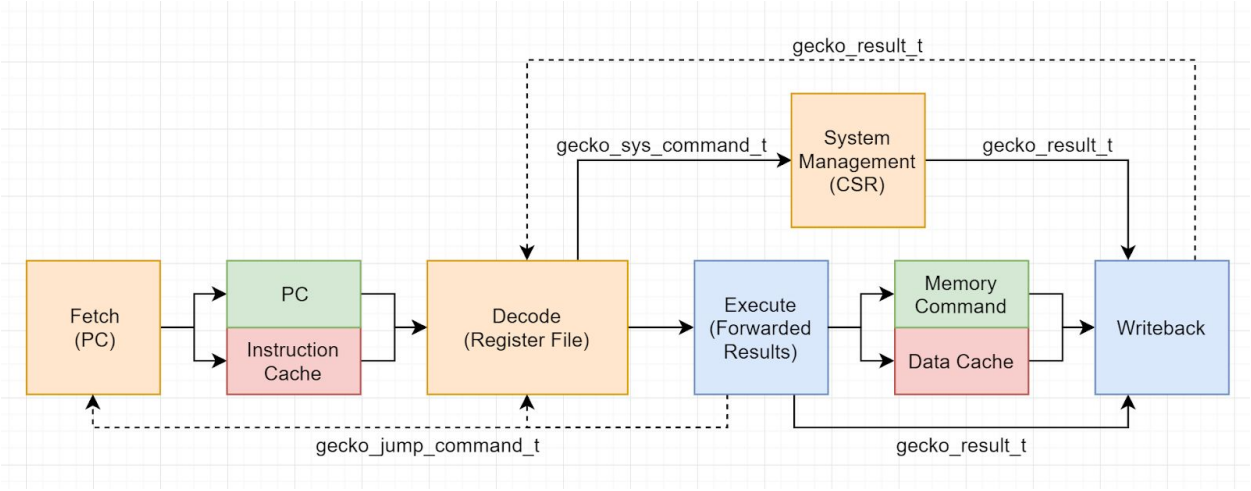
This week I worked on writing more logic for the RISC-V core, which included finishing the writeback stage and starting to write more logic for the decode stage, which in the current architecture is one of the most complicated modules. I also moved the system management module containing the control and status registers out of the execute stage to simplify my design.



Forwarding in this architecture works a little differently due to the routing concerns in the FPGA, with no direct forwarding of results from stages to the decode module. Instead two different modifications are made to improve IPC while also not creating excessive links between stages. First, the execute stage stores the last result it generated, so sequentially dependent ALU operations can be sent along from decode, with a flag indicating their results exist later in the pipeline. Second, execute can send its results past the memory stage if it is doing an ALU operation and not computing a memory address, which allows for the execute value to get written back a cycle faster than a usual five-stage pipeline.

Along with the other members of my group we also did some collective brainstorming on different programs we can run on our architecture to prove its effectiveness, and we think ray-tracing a simple scene may give us another data-point to justify the usefulness of our architecture.