Project Status Report #2
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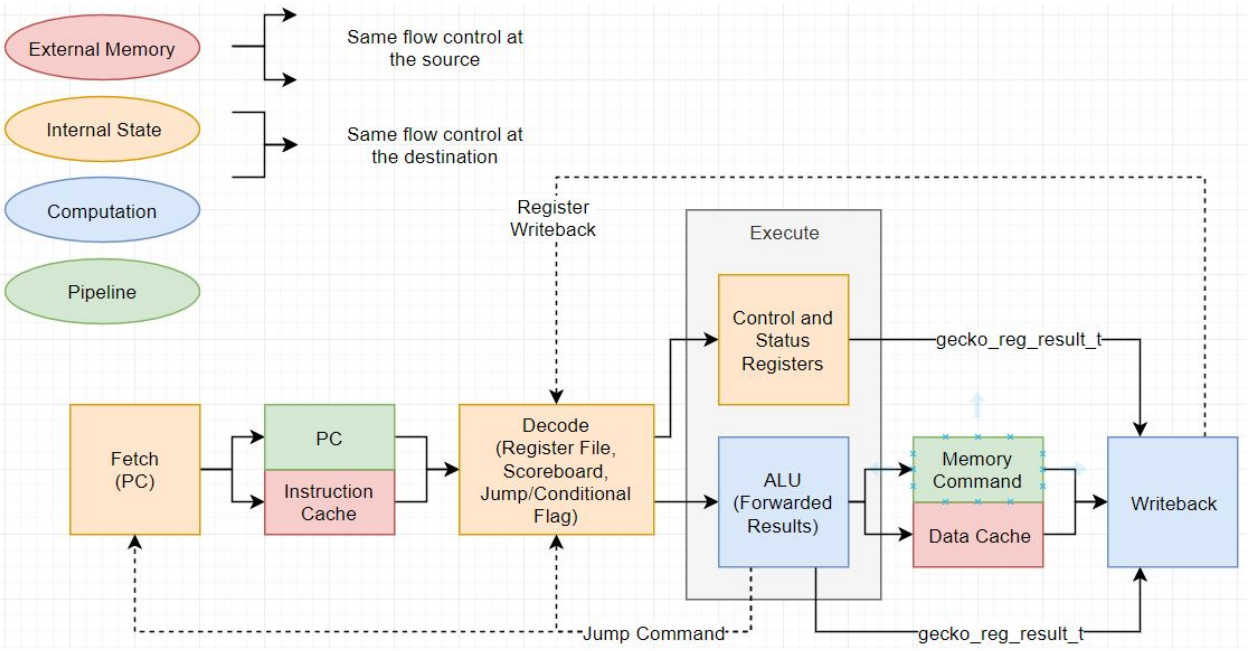
This week I worked on further improving the design of the lightweight RISC-V core for running the vector co-processor. Over last week I moved the memory access to after the ALU, while still providing a datapath straight from the ALU to the writeback stage. Of note is my focus on making sure that the flow control on the core is distributed in each module without a central control module, which allows arbitrary pipeline stages to be placed in the pipeline to increase timing while sacrificing a slight amount of IPC. This is critical in an FPGA, since routing delays are one of the biggest hazards to clock frequency, especially when the clock-enables on every register in your CPU can depend on a single back-flow signal from the very last pipeline stage.



I am slightly delayed in finalizing the implementation of the core, mostly from being sick, but I am hoping to have it working this week at the latest. I also worked with Cyril on helping him implement some of the floating point resources some more, and at the beginning of the week handed off to Alex all of the necessary repositories he needed to get the compiler working.