Cyril Agbi (cyrila) Team: A3

18500: Capstone Log

WEEK	Task(s) Completed	Status	Comments
Jan. 20-26	- Reused/edited FPU adder from 18340 - Reused/edited FPU multiplier from 18340	On time	
Jan. 27 - Feb. 2	- Made a FPU square root module - Discussed with David about optimizing the FPU for the FPGA - Created a rough FPU block diagram	On time	*Need to test for correctness more vigorously *The square root module does not handle denormal numbers well
Feb. 3-9	- Made a FPU division module - Read assigned reading for Capstone - Made a program to randomly generate FPU test cases - Debugged division module	One time	*Division Module has multiple errors [FIXED 2/7/19] **NOTE: the current tests show some of the FPU results to be very slightly off.
Feb. 10-16	- Met with David to learn/discuss how to rewrite the FPU in terms of System Verilog functions - Started to functionalize modules (Functionalized division and multiplication)	A little behind	*Needed to spend time on other classes *Make rounding function for FPU
(Feb. 17-23)	- Finish rewriting FPU in terms of functions - Test/debug the FPU - Work out a better way to pipeline FPU	n/a	*Might not really get into pipeline until next week