Cyril Agbi Capstone: Team A3

LOG: 2/17/19 – 2/23/19

I finished turning the FPU modules into functions. This will make it easier for Vivado to synthesize the FPU. It will also make it easier to understand the code.

I have two implementations of a divider. The one that I am working with right now is the pencil-paper method that we know of (restoring division). However, this will make division slow because it needs to do up to 46 subtractions, and each subtraction is dependent on the last. The other implementation that I have also uses the restoring division method. However, it allows us to use some bit manipulation tricks in order to do division. Both implementations would take up to 46 cycles to complete (if pipelined), but it would be a lot easier to implement the second method with pipelining.

David explained to me that there are these special units on the FPGAs called DSP (digital signal processing) slices. These DSP slices are pieces of dedicated hardware designed by the FPGA designers with the sole purpose of doing arithmetic. So, if we can get the Vivado synthesize tool to use these slices, we should be able to speed up some operations. The issue is that the DSP slices on our board can only do 27-bit by 18-bit multiplication. Therefore, we need to figure out a way to make do 24-bit by 24-bit multiplication.

For next week, I would like to test out the use of these DSP slices on the FPU addition operation. If that goes well, I will attempt to modify multiplication as well. I will also like to test the pipeline that I have laid out for the FPU.