	Project Proposal		Design Presentation					Interim Demo			Final Presentation	
TASK TITLE	W4	W5	W6	W7	W8	W9	W10	W11	W12	W13	W14	W15
	9/20	9/27	10/4	10/11	10/18	10/25	11/1	11/7	11/15	11/22	11/29	12/6
Hardware												
Get Hardware												
Acquire Ultra96	JSG											
Acquire Peripherals	JSG											
Ramp on Ultra96												
Research I/O	JSG	JSG	JSG									
Initial Host/Fabric communications		JSG										
Write (initial) SRCNN model in HW												
Write convolution kernel in Vitis HLS				JSG	JSG	JSG	JSG	JSG				
Write general CNN in Vitis HLS									JSG			
Fit full-sized model on the board in Vitis									JSG			
Optimise tile sizes									JSG	JSG	JSG	JSG
Speed up w/ HLS pragmas									JSG	JSG	JSG	JSG
Accomodate Switch to New Model												
Rewrite CNN											JSG	
Specialize CNN											JSG	
Final Model Attempt												
Setup xfopencv in Vitis												JSG
Benchmark functions												JSG
Implement FSRCNNs												JSG
Validate HW implementation												JSG
Benchmark HW implementation												JSG
Validate HW Algorithm												
Port SW model onto FPGA									JSG	JSG		
Validating FPGA model against SW model										JSG	JSG	JSG
Time Benchmarking							JSG	JSG	JSG	JSG	JSG	JSG
User Experience												
UI								KB	KB	KB	KB	KB
Command Line UI												JSG
Display to screen			KB	KB	KB	KB	KB	KB	KB	KB	KB	JSG
Test screen display								JSG	JSG	JSG	JSG	JSG
Read video from storage device			KB	KB	KB	KB	KB	KB	KB	KB	KB	JSG
Test video reading								JSG	JSG	JSG	JSG	JSG
Research CAD Design for FPGA Holder									JSG	JL		
Create Holder for FPGA										JL		
Software												
Model Research												
Research DSP vs CNN models	ALL							ALL				
Research specific CNN models		JL	JL									
Benchmark CNN Models		JL	JL	JL								
Metric Research												
Research VMAF	JL	JL										
Benchmark VMAF		JSG										
Research SSIM	JL											
Benchmark SSIM		JL										
Setup training infrastructure												
Acquire AWS Credits		KB	KB	KB	KB	KB						
Setup AWS		KB	KB	KB	KB	KB						
Acquire Dataset	JL											
Setup CoLab							JL	JL				
Model Training												
Develop Python Code for Training			JL	JL	JL							
Run Training				JL	JL	JL	JL					
Test/Evaluate Model				JL	JL	JL	JL			JL	JL	JL
Finalize model hyperparameters							JL					
Further optimizing weights							JL	JL	JL	JL	JL	JL
Milestones												
Proposal Presentation	JSG											
Design Presentation			KB									
Design Review Report			ALL	ALL								
Interim Demo							JL, JSG	JL, JSG				
FInal Video												JL
Final Presentation											JL	JL

Initials (Lead)
JSG = James
JL = Josh
KB = Kunal

Colours (Progress)
Green = Complete
Yellow = Partial
Red = None